

BANDGAP VOLTAGE REFERENCE USING TRIPLE CASCODE OPERATIONAL AMPLIFIER

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Abstract

Bandgap Voltage reference (BGR) circuits are crucial components in analog circuits. In this paper, a BGR circuit capable of obtaining a reference voltage of 1.0435 V is proposed. In the proposed BGR circuit, Miller compensated two-stage Triple Cascode Operational Amplifier (Op-Amp) has been used which achieves a higher gain of 104.1db and Phase Margin of 73.78 degrees with 1.8V supply voltage using 90nm technology. The proposed BGR circuit achieves 4.51 ppm/OK of temperature coefficient and 0.4375 mV/V of line regulation. The designed BGR circuit can be used in analog applications.

Keywords: Bandgap Voltage Reference; Gain; Miller compensation; MOSFET; PM; Temperature coefficient; Triple Cascode Op-Amp

Introduction

Voltage reference sources are indispensable for providing a precise and stable voltage signal despite temperature fluctuations, variations in supply voltage, and process deviations (Lin and Lin, 2006; Baker, 2019; Chowdary *et al.*, 2020; Azimi *et al.*, 2021; Aminzadeh and Valinezhad, 2022). Recent advancements in voltage reference circuits have focused on minimizing area without resorting to resistors (Wang and Mok, 2020; Chen *et al.*, 2024), and operating at low supply voltage levels, such as 1 V (Banba *et al.*, 1999; Serra-Graells and Huertas, 2003; Wang *et al.*, 2018; Osaki *et al.*, 2020; Banerjee *et al.*, 2024). However, these methods frequently require Bipolar Junction Transistors (BJTs), which have a significant turn-on voltage, reaching up to 0.6 V at room temperature (Shrivastava *et al.*, 2015; Mu *et al.*, 2017).

There have already been multiple research studies reported on the Operational amplifier (Op-Amp) and Bandgap Voltage reference (BGR) circuits (Li *et al.*, 2011; Adimulam and Movva, 2012; Singh *et al.*, 2015; Liu *et al.*, 2018a; Liu *et al.*, 2018b; Kaur *et al.*, 2019; Nagulapalli *et al.*, 2019, 2021; Shashidhar *et al.*, 2020; Guo and Qiu, 2023; Banerjee *et al.*, 2024). For example, Guo *et al.* investigated a double cascode circuit without any compensation and obtained a poor gain of 50 dB but higher stability (i.e., a phase margin of 75 degrees). Moreover, Nagulapalli *et al.* used Miller compensation, resulting in a 10 dB improvement in gain without degrading the stability. Finally, Shashidhar *et al.* designed a folded cascode Op-Amp to improve stability (i.e., a phase margin of 68.89 degrees) without affecting the gain. Liu *et al.*

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investigated subthreshold region Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and obtained a high temperature coefficient of 34 ppm/OK and 82 ppm/OK. Nagulapalli *et al* eliminates one current mirror stage and obtained a temperature coefficient of 24.4 ppm/OK. First order compensation can only decrease the temperature coefficient (TC) of output voltage to about 13ppm/OK in the presence of nonlinearity.

In this work, the design and simulation of a two-stage triple cascode Op-Amp with RC Miller compensation have been performed. However, the gain and stability can be significantly improved by using cascoding technique. The BGR circuit using triple cascode Op-Amp is designed and simulated to obtain stable output reference voltage with comparable temperature coefficient and line regulation.

Section II provides the methodology followed to design the proposed Triple Cascode Op-Amp. Section III shows the design of proposed BGR circuit. Section IV outlines the comparison of various parameters that are evaluated after simulations, while Section IV concludes the study.

Materials and Methods

Proposed Operational Amplifier

The Bandgap circuit requires an Op-Amp with high gain and bandwidth to achieve desired characteristics (Hamzah *et al.*, 2015; Soni *et al.*, 2022; Sousa *et al.*, 2022). For attaining substantial gain and broad bandwidth in Op-Amp configurations, the conventional approach involves employing a two-stage RC Miller-compensated Op-Amp (Khan *et al.*, 2021; Aggarwal *et al.*, 2022; Manikandan, 2024). In this technique, a compensation capacitor (C_C) and nulling resistance (R_Z) is inserted between the input and output of the IInd stage. The inclusion of this resistor aids in regulating the gain over the right-half plane (RHP) zero, thus enhancing the stability of the Op-Amp (Palumbo and Pennisi, 2002). To mitigate the RHP zero, R_Z should follow the equation 1 or relocate from the RHP to the left-half plane (LHP), positioned above the second pole. When R_Z is increased to an infinite value, the compensation network becomes an open circuit, preventing pole splitting.

$$R_Z = \frac{1}{g_{m2}} = \left(\frac{C_C + C_L}{C_C} \right) * \frac{1}{g_{m2}} \quad (1)$$

Where, g_{m2} , C_L represents the transconductance of the second-stage amplifier and load capacitor respectively. The proposed Op-Amp design as

shown in Figure 1 integrates a Triple Cascode Telescopic input in the initial stage to achieve significant gain, while a common-source amplifier in the output stage facilitating substantial voltage swing. The aspect ratio of the transistor (W/L) is a critical parameter influencing the performance of the transistor. It is determined based on the desired drain current (I_D) and other circuit requirements. The aspect ratios of the proposed Op-Amp are tabulated in Table 1. The cascoding technique effectively elevates the output impedance at the output stage, consequently enhancing the overall gain of the Op-Amp (Razavi, 2017). The biasing supply voltage at the gates of transistors (M3, M4) and (M5, M6) is 650mV and 800mV respectively for the proposed Op-Amp. The design specifications and simulated results are summarized in Table 2.

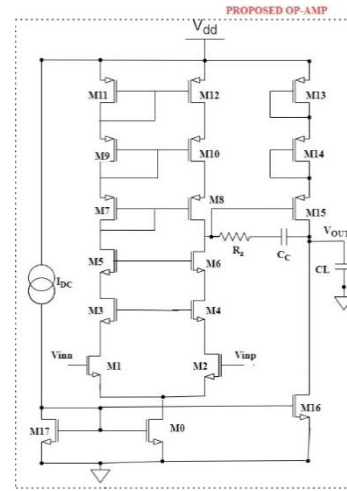


Figure 1. Architecture of Proposed Miller Compensated Triple Cascode Op-Amp

Table 1. Aspect ratios of the proposed op-amp

Transistors	Aspect ratio (W/L)
M1, M2, M3, M4, M5, M6	4μm/500nm
M7, M8, M9, M10, M11, M12	3μm/500nm
M13, M14, M15	22μm/500nm
M16	23μm/500nm
M0	8μm/500nm

Table 2. Design specifications and simulated results of the proposed op-amp

S.NO	Parameters	Specifications
1.	Supply Voltage	1.8V
2.	Technology	90nm
3.	Load Capacitance (C_L)	1pF
4.	Nulling Resistor (R_Z)	15kΩ
5.	Compensation Capacitor (C_C)	0.75pF
6.	Open loop gain (dB)	104.1
7.	Phase margin (degree)	73.78
8.	Gain Bandwidth Product (MHz)	30.90
9.	CMRR (dB)	87.28

The proposed Op-Amp has attained a higher gain of 104.1dB as shown from Figure 2. The graph shows gain as a function of frequency, which is a characteristic of an Op-Amp. The gain is enhanced due to the increased impedance at the output stage due to cascoding of transistors. The variation of phase plotted against frequency is shown in Figure 3. From the graph, it is evident that the Op-Amp does not introduce a significant phase shift at low frequencies.

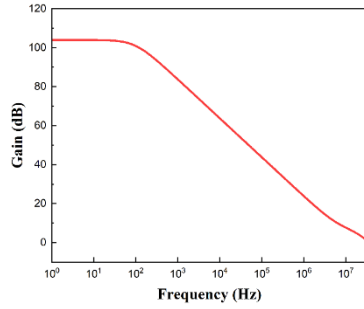


Figure 2. Variation of Open Loop Gain vs Frequency

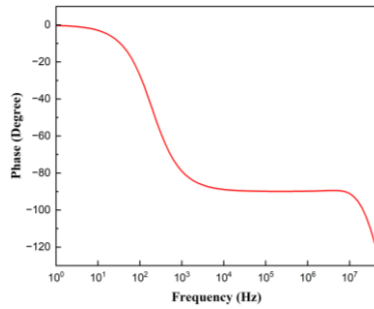


Figure 3. Variation of Phase vs Frequency

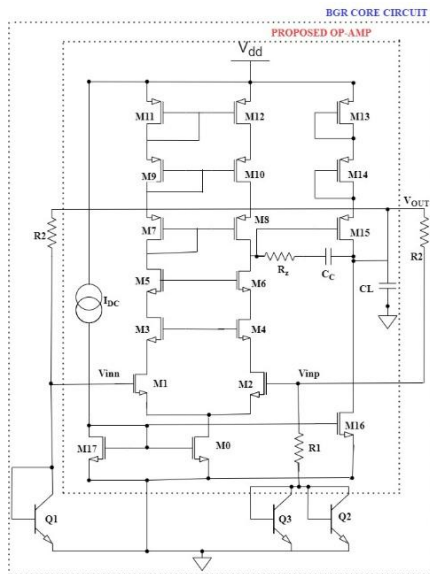


Figure 4. Architecture of Proposed BGR Circuit using Triple Cascode Op-Amp

Proposed Bandgap Voltage Reference

The BGR circuit of the proposed design is shown in Figure 4. The BGR circuit needs an Op-Amp with high DC gain making good virtual ground between the two nodes. The complementary-to-absolute-temperature (CTAT) voltage in the BGR circuit is generated by the base-emitter voltage (V_{BE}) of a BJT, while the proportional-to-absolute-temperature (PTAT) voltage is produced by the thermal voltage (V_T) derived from the VBE of two BJTs operating at different current densities. The thermal voltage (V_T) is a physical constant that represents the voltage corresponding of thermal energy in a semiconductor device.

$$V_{REF}(T) = V_{BE}(T) + MV_T(T) \quad (2)$$

Differentiating the above Equation with respect to the temperature yields:

$$\begin{aligned} \frac{\partial V_{REF}(T)}{\partial T} &= \frac{\partial (V_{BE}(T) + MV_T(T))}{\partial T} \\ &= \frac{\partial V_{BE}(T)}{\partial T} + M \frac{\partial V_T(T)}{\partial T} \end{aligned}$$

Noted that,

$$\begin{aligned} \frac{\partial V_{BE}(T)}{\partial T} &= -1.73 \text{ mV/K} \\ \frac{\partial V_T(T)}{\partial T} &= 0.09 \text{ mV/K}. \end{aligned}$$

Therefore, the optimal M at $T = T_{(nom)}$ obtained by evaluating

$$\begin{aligned} \frac{\partial V_{REF}(T)}{\partial T} \bigg|_{T=T(nom)} = 0 \text{ yields} \\ M = - \frac{\partial V_{BE}(T)/\partial T}{\partial V_T(T)/\partial T} \bigg|_{T=T(nom)} = \frac{-1.73}{-0.09} = 19.22. \end{aligned}$$

This way by properly choosing the area multiplicity factor 'M' and value of resistance R2, first order temperature dependency in these two CTAT and PTAT voltages is cancelled out, resulting an almost temperature independent voltage source.

$$I_D = \frac{V_T \ln(N)}{R1} \quad (3)$$

where N represents the ratio of the emitter area of Q2 to Q1.

This circuit produces the output voltage (V_{REF}):

$$V_{REF} = V_{BE} + \left(\frac{R2}{R1}\right) \ln(N)V_T \quad (4)$$

In equation (4), the VBE term corresponds to the CTAT voltage, while the VT term represents the PTAT voltage. The resistor values and N should be chosen such that the temperature effects of the CTAT and PTAT voltages offset each other. The value of R1 and R2 can be calculated from the (3) and (4) respectively. The design specifications of the proposed BGR circuit are summarized in Table 3.

Table 3. Design specification of the proposed BGR circuit

Transistors	Aspect ratio (W/L)
M1, M2, M3, M4, M5, M6	4 μ m/500nm
M7, M8, M9, M10, M11, M12	3 μ m/500nm
M13, M14, M15	22 μ m/500nm
M16	23 μ m/500nm
M0	8 μ m/500nm

Result and Discussion

This section delves into the simulated results of the proposed BGR circuit using the Cadence Virtuoso tool at 90 nm CMOS technology (Lopez Martin, 2002; Cadence Design Systems, 1988). Figure 5 illustrates the output voltage (V_{ref}) plotted against temperature at a 1.8V supply voltage. The graph shows that a V_{REF} of 1.0435V is produced at room temperature (25°C) for the Typical (TT) process corner. The total voltage variation is relatively small, indicating that V_{REF} remains stable over a wide temperature range. Within a temperature span of -10°C to 110°C, the observed voltage variation is only 0.20 mV, yielding an impressively low Temperature Coefficient (TC) of 4.51 ppm/°K.

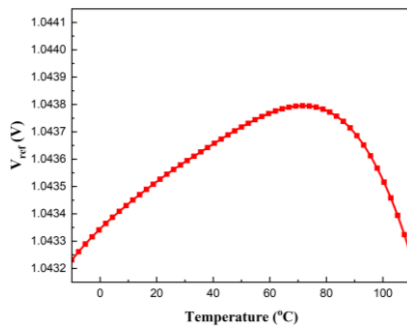


Figure 5. Variation of Output Voltage vs Temperature

The variation of V_{REF} plotted against supply voltage at room temperature is shown in Figure 6. The flat region beyond 1.5V suggests a well-regulated V_{REF} , a crucial characteristic for stable

electronic systems. This indicates that the BGR circuit is properly regulated and independent of increase in supply voltage. The line sensitivity is recorded to be 0.4375mV/V in the supply voltage range spanning from 1.8V to 5 V.

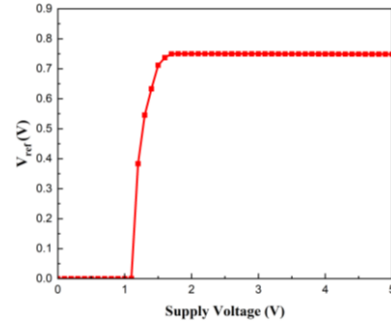


Figure 6. Variation of Output Voltage vs Supply Voltage

To ascertain the robustness of the proposed design under varying conditions, Monte-Carlo simulations were executed on 10 samples, examining the output voltage. Figure 7 shows the variation of V_{REF} with temperature for 10 different simulation samples (S1 to S10). The V_{REF} variation among samples is minimal, staying within a narrow range of approximately 1.040V to 1.047V. Further, Figure 8 depicts the variation of the V_{REF} with supply voltage for 10 different simulation samples (S1 to S10) which shows the consistent behavior of V_{REF} across all samples. However, a minor variations in the behavior of V_{REF} can be seen in the results due to process variations. The comprehensive performance evaluation is provided in Table 4, offering a comparative analysis with recent works on BGR. The proposed circuit has a minimum temperature coefficient and line sensitivity as compared to other conventional BGR circuits due to use of the cascoding technique in the Op-Amp.

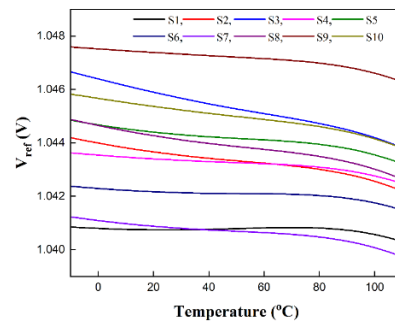
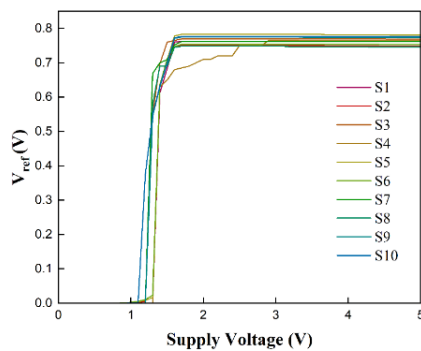


Figure 7. Variation of Output Voltage vs Temperature for 10 samples

Table 4. Performance comparison with recent works of bandgap voltage reference

	This work	Banerjee <i>et al.</i> (2024)	Liu <i>et al.</i> (2018a)	Liu <i>et al.</i> (2018b)	Nagulapalli <i>et al.</i> (2021)	Adimulam and Movva (2012)	Singh <i>et al.</i> (2015)	Kaur <i>et al.</i> (2019)	Li <i>et al.</i> (2011)
Technology (μm)	0.09	0.18	0.18	0.18	0.045	0.065	0.032	0.18	0.05
Vref (V)	1.0435	0.607	0.755	0.210	0.5	0.540	0.725	0.789	1.2
TC (ppm/ $^{\circ}\text{C}$)	4.51	57	34	82	24.4	1.8%	13	71.69	8.9
Temperature range ($^{\circ}\text{C}$)	-10 to 110	-40 to 85	-15 to 140	-40 to 140	-40 to 120	-40 to 125	-40 to 100	-40 to 125	-40 to 110
Line Regulation (mV/V)	0.4375	0.80	2.8	0.27	1.5	N.A.	N.A.	N.A.	2.4
Supply Voltage (V)	1.8	1.8	1.1	0.4	1.05	1.2	1.8	1.8	1.8

**Figure 8. Variation of Output Voltage vs Supply Voltage for 10 samples**

The cascoding technique used in Op-Amp helps in the reduction of channel length modulation thereby suppressing the current mismatch in the two branches of the BGR circuit. It also helps in dealing with gain stability trade off present in the conventional BGR circuit. The design excels in achieving a well-balanced performance across various metrics, including the technology, temperature coefficient, temperature range, and line sensitivity.

Conclusion

This paper presented the design and simulation of Miller compensated Triple Cascode Op-Amp and BGR circuits at 90nm technology. The cascoding technique used in Op-Amp helps in reduction of channel length modulation and deals with gain stability trade off present in the conventional BGR circuit. The proposed circuit has impressive TC and line regulation making it a very attractive choice for analog applications.

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