

PERFORMANCE ENHANCEMENT OF BULK-DRIVEN QFG MOSFET LOW VOLTAGE CASCODE CURRENT MIRROR

Mohd Javed, Rockey Gupta, and Susheel Sharma*

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Abstract

Bulk-driven (BD) and Floating gate (FG) MOSFET are commonly used in applications where power consumption and voltage levels are relatively low due to their simplicity and efficiency. However, some drawbacks, such as reduced linearity and stability in the BD technique and reduction of transconductance in FG techniques, can be addressed by amalgamating both FG and BD techniques. This paper evaluates the performance of a bulk-driven quasi-floating gate (BDQFG) cascode current mirror circuit in comparison to a quasi-floating gate (QFG) and bulk-driven quasi-floating gate (BDQFG) current mirrors. The findings show that the BDQFG cascode current mirror offers an output resistance of 2.78 M Ω , an input resistance of 3.71 k Ω with a bandwidth of 664.5 MHz, and a current transfer ratio of 0.99. The bandwidth is further improved to 1.4 GHz and 1.93 GHz in subsequent modifications. The workability of the proposed circuits has been demonstrated using a $\pm$ 0.5 V power supply in a 130 nm CMOS technology. The design has been verified through simulation using PSpice.

Keywords: Bulk-driven MOSFET; Cascode current mirror; Floating gate MOSFET

Introduction

The design of low-power and low-voltage analog circuits is crucial in the current trend toward smaller and more portable electronic devices. The primary challenge in this design is to maintain the performance characteristics while operating at low voltage levels with minimum power consumption. High transistor threshold voltage poses a significant challenge for researchers. In VLSI design, a current source is often necessary, where the current mirror is employed as a unity gain current amplifier that provides an output current proportional to the input current at a high output impedance. It is desirable to

have an output current independent of the output node voltage with unity current mirror gain constant across all frequencies.

To address the low-voltage and low-power design challenge, several traditional and unconventional techniques have been developed. Traditional methods such as the level shifter (Rajput and Jamuar, 2002), the flipped voltage follower (Ramírez *et al.*, 2002), the subthreshold operation (Allen *et al.*, 2002), dynamic threshold MOSFET (Jang *et al.*, 2010), and self-cascode (Sanchez-Sinencio, 2000) have been used to minimize the

Department of Electronics, University of Jammu, Jammu, Jammu and Kashmir 180006, India.
Email: mohd.javed@jammuuniversity.ac.in; rockygupta@jammuuniversity.ac.in; susheelsharma@gmail.com*

* Corresponding author

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current mirror's input compliance voltage, improve its output impedance, and reduce power dissipation.

The unconventional techniques, such as BD (Blalock *et al.*, 1995, 1998; Chang *et al.*, 2013), floating-gate (Ziegler *et al.*, 2016; Sharma *et al.*, 2006; Ramirez *et al.*, 1995; Aggarwal and Gupta, 2009), quasi-floating-gate (Angulo *et al.*, 2004), BD floating-gate (Khateb *et al.*, 2014), and BD quasi-floating-gate (Javed *et al.*, 2023; Khateb, 2015), offer reduced structural complexity with a wider input voltage operating range, thus providing a more attractive solution for low-voltage and low-power analog circuit design.

Despite these advantages, the unconventional methods still exhibit low transconductance, which leads to a lower gain-bandwidth product and higher input-referred noise (Khateb *et al.*, 2013). The floating-gate approach also increases the silicon area requirement due to its large capacitance (Sharma *et al.*, 2006; Ramirez *et al.*, 2003), and it may trap a large quantity of charge during fabrication, resulting in offsets. BDQFG MOSFETs address these issues by offering a higher transconductance value, which is the sum of the transconductance of BD and QFG MOSFETs (Khateb and Khatib, 2011; Khateb *et al.*, 2014).

The quasi-floating-gate MOSFETs have also been developed to address the limitations of floating-gate MOSFET based devices with enhanced gain bandwidth product and reduced input-referred noise (Ren *et al.*, 2005; Torralba *et al.*, 2009). In this paper, we have employed a cascode connection in the QFG MOSFET current mirror, whereas the current mirror section transistors operate in bulk mode.

Low Voltage Low Power Techniques

Bulk-driven MOSFET

In 1987, Guzinski *et al.* introduced the concept of the BD MOSFET, which has since been widely used for designing various analog building blocks (Zhang and Masry, 2004; Chatterjee *et al.*, 2005; Haga *et al.*, 2009a; Haga *et al.*, 2009b; Vlassis and Raikos, 2009; Raikos and Vlassis, 2010; Khateb and Khatib, 2011). In the bulk-driven method, a bias voltage is employed on the MOSFET's gate, and the signal is applied at the terminal, which keeps the channel unchanged until the gate bias voltage is constant. This removes the threshold voltage restriction on the signal pathway and makes it possible to expand the range of low supply voltage applications for any analog circuit.

The threshold voltage of the BD MOSFET is given as:

$$V_{TH(VB'S)} = V_{tho} + \gamma\sqrt{2\phi_F + V_{BS}} - \gamma\sqrt{2\phi_F} \quad (1)$$

Drain current can be expressed as:

$$i_D = k \frac{W}{L} (V_{GS} - V_{TH(VB'S)})^2 \quad (2)$$

The transconductance of bulk-driven MOSFET is given by:

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{BS}}} \quad (3)$$

where γ is bulk threshold parameter and $2\phi_F$ is surface potential at strong inversion. g_{mb} represents the transconductance from the bulk input node voltage V_{BS} to the output current i_{ds} .

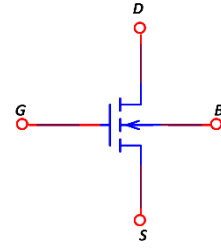


Figure 1. Symbol of BD MOSFET

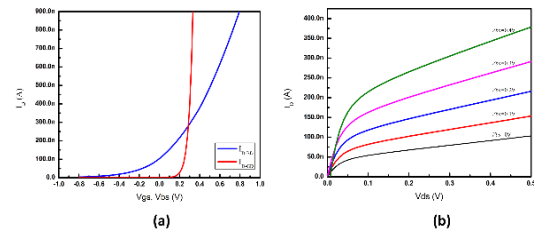


Figure 2. (a) Transfer characteristic (b) Output characteristic of BD MOSFET

N-channel BD MOSFET shown in Figure 1 has been simulated by PSpice with 0.5 V supply voltage and the aspect ratio taken as $2.6 \mu\text{m}/0.13 \mu\text{m}$ for obtaining the transfer and drain characteristics. The comparative transfer characteristics and the output characteristics of BD MOSFET and conventional gate-driven MOSFET are shown in Figures 2(a) and 2(b), respectively. As evident from Figure 2(a), in BD MOSFET, the threshold voltage is significantly lower than in conventional MOSFET. This is because the channel in a BD MOSFET is formed in the bulk region, which is inherently more

conductive than the lightly doped channel region in conventional MOSFET. As a result, the transfer characteristic of a BD MOSFET is nonlinear, and the device can be turned ON with lower gate voltage, which makes it more suitable for low-power applications. Figure 2(b) shows the output characteristics of BD MOSFET, which shows the effect of bulk-source voltage on the drain current.

Bulk-Driven Quasi-Floating Gate MOSFET

Quasi-floating gate MOSFETs have been developed to address the limitations of the FGMOS-based architecture. The structure of a QFGMOS is similar to that of a floating gate MOSFET, with the signal inputs of the quasi-floating gate MOSFET being connected through capacitance to the floating gate, which in turn is connected to the supply voltage through a transistor operating in the cutoff region (Rodriguez-Villegas, 2006; Sharma *et al.*, 2006). This modification of the floating gate MOSFET structure improves the overall performance of the QFGMOS, and it has been employed as analog building blocks such as current conveyors, current mirrors, and current dividers (Angulo *et al.*, 2004; Moradzadeh and Azhari, 2011; Gupta and Sharma, 2012; Pandey and Kiran, 2020).

The effective transconductance of QFG MOSFET can be calculated as follows:

$$g_{m,eff} = g_{m,fg} \frac{C_{in}}{C_{Total}} \quad (4)$$

The use of the bulk-driven approach has resulted in significant improvements in the linearity, attainable gain, and supply voltage characteristics of analog circuits, making it suitable for applications such as current mirrors (Raj *et al.*, 2016; Bchir *et al.*, 2020), and operational amplifier circuits (Dubey and Bhadauria, 2019). Despite its benefits, the bulk-driven method is still limited by its relatively low transconductance and excessive input-referred noise. However, by combining the bulk-driven

approach with the quasi-floating gate technology, a new device known as the BDQFG MOSFET has been created, which boasts a higher transient frequency and transconductance compared to other low-voltage techniques while also eliminating the need for a threshold voltage requirement in the signal path. Figure 3 shows the symbol and equivalent circuit of a BDQFG MOSFET. The circuit is a combination of a QFG MOSFET and a BD MOSFET.

The drain current of BDQFG MOS can be expressed as:

$$i_{D,BD-QFG} = (i_{D-bulk} + i_{D-QFG}) \quad (5)$$

where, $i_{D-bulk} = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{TH(VB'S)})^2$ and

$$i_{D-QFG} = \frac{1}{2} \mu_0 C_{ox} \left(\frac{W}{L} \right) \left[\left(\frac{C_{in}}{C_{Total}} V_{in} + \frac{C_{gd}}{C_{Total}} V_{bias} \right) - V_T \right]^2$$

The transconductance of BDQFG MOS can be calculated as:

$$g_{m,BD-QFG} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{BS}}} + \mu_0 C_{ox} \frac{W}{L} \left(\frac{C_{in}}{C_{Total}} V_{in} + \frac{C_{gd}}{C_{Total}} V_{bias} - V_T \right) \frac{C_{in}}{C_{Total}} \quad (6)$$

The effective transconductance of BDQFG MOS is denoted by the expression:

$$g_{m,BD-QFG} = g_{mb} + g_{m,eff} \quad (7)$$

As evident, the transconductance ($g_{m,BD-QFG}$) of a BDQFG MOSFET (eqn. 7) is higher than that of a BD MOSFET (eqn. 3) and QFG MOSFET (eqn. 4). This is because the BDQFG MOSFET combines the conductive channel in the bulk region of the BD MOSFET with the floating gate structure of the quasi-floating gate MOSFET. The resulting device structure provides a larger gate-to-bulk capacitance and enhanced gate control over the channel, which leads to a higher transconductance. Additionally, the BDQFG MOSFET allows for greater control of the floating gate potential, which further enhances the transconductance of the device. The higher transconductance of the BDQFG MOSFET makes it suitable for applications that require high-performance analog circuits.

Further, the transition frequency of BDQFG MOSFET, as reported by Khateb (2014), is:

$$f_{T,bd-qfg} = \frac{g_{m,bd-qfg}}{2\pi(C_{bs} + C_{fgs})} \quad (8)$$

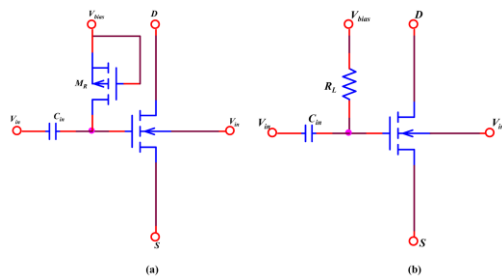


Figure 3. (a) BDQFG MOSFET symbol and (b) its equivalent

The transient frequency BDQFG (eqn. 8) is higher than BD and QFG MOS but still lesser than gate-driven MOS devices, as reported by Khateb *et al.* (2014). $g_{m, bd-qfg}$ is the effective transconductance of BDQFG MOSFET and C_{bs} , C_{fgs} are bulk-source and gate-source parasitic capacitances, respectively.

Design of low-voltage current mirrors

QFG MOSFET current mirror

A QFG MOSFET current mirror circuit is depicted in Figure 4. As a result of the reduced effective threshold voltage of QFG MOSFET, it is suitable for low-voltage applications. In this configuration, a high value resistor implemented through M_p weakly connects the MOSFET gates (M_1 , M_2) to the supply rail (Gupta and Sharma, 2012).

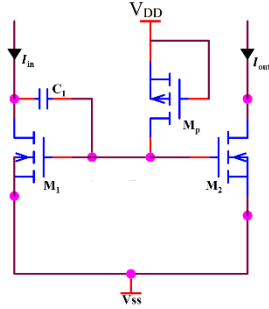


Figure 4. QFG MOSFET current mirror circuit

BDQFG MOSFET current mirror

The Bulk-driven version of the QFG MOSFET current mirror is shown in Figure 5, which is expected to improve the current mirror accuracy and bandwidth.

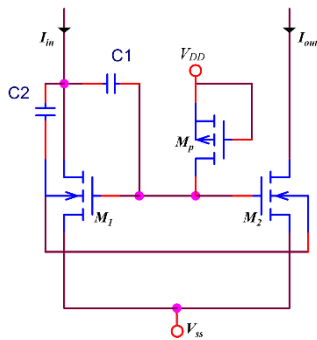


Figure 5. BDQFG current mirror

In the context of the comparative transfer characteristics depicted in Figure 2(a), it is evident that the threshold voltage (V_{th}) of the BD MOSFET is lower than that of the gate-driven MOS transistor.

Consequently, the BDQFG current mirror incorporates transistors with lower V_{th} values, facilitating a broader compliance voltage range. This expanded operational range enables the current mirror to function effectively at lower input voltages. Conversely, the QFG MOSFET current mirror employs transistors with higher V_{th} values, which restricts its compliance voltage range compared to the BDQFG current mirror, as illustrated in Figure 6. Both QFG and BDQFG current mirror circuits demonstrate a stable output current across the output voltages, with the BDQFG exhibiting a wider compliance range compared to the QFG MOSFET. The improved performance of the BD-QFG, particularly its broader compliance range is attributed to the bulk-driven technique, which enhances linearity and extends the usable voltage range compared to the standard QFG MOSFET.

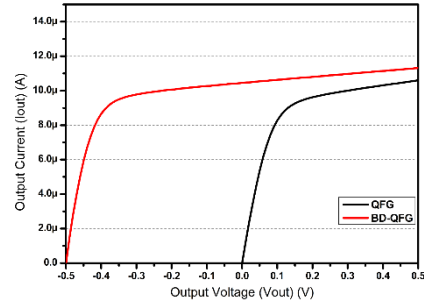


Figure 6. Output compliance voltage of QFG and BDQFG current mirror

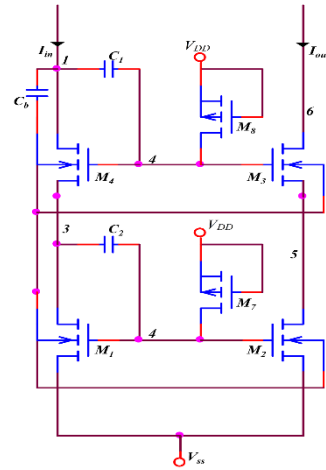


Figure 7. BDQFG cascode current mirror

BDQFG cascode current mirror

The design of a low-voltage BDQFG cascode current mirror is shown in Figure 7. In this configuration, M_1 and M_2 form the basic current mirror, whereas M_3 and M_4 form cascode

configuration. All the devices in this circuit are in bulk-driven configuration via a capacitor C_2 except M_{p1} and M_{p2} . The MOS M_{p1} and M_{p2} are used to connect the gates of M_1 , M_2 , M_3 , and M_4 to supply rail for QFG operation. This setup significantly enhances the accuracy of the current mirroring and transfer ratio compared to the QFG and BDQFG approaches. The addition of cascoding also results in an increased output resistance. Specifically, the output resistance of the BDQFG gate cascode current mirror is found to be $2.78 \text{ M}\Omega$, which is higher than that of the quasi-floating gate ($181 \text{ k}\Omega$) and the BQFG current mirror ($157 \text{ k}\Omega$). However, its bandwidth is smaller compared to that of the QFG and the BDQFG current mirror due to the large input capacitance.

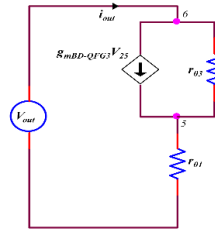


Figure 8. Small signal model of BDQFG cascode current mirror for output resistance

Small signal analysis of BDQFG cascode current mirror

Resistance at output node: The output resistance directly impacts the current mirror's accuracy by defining how sensitive the output

current (I_{out}) is to changes in the output voltage (V_{out}). A high output resistance is particularly valuable as it minimizes the variations in the mirrored current when the load voltage changes. The small signal model of the BDQFG cascode current mirror for calculating output resistance is shown in Figure 8.

The output resistance obtained is expressed as:

$$r_{out} = \frac{V_{out}}{i_{out}} = r_{03} + r_{01} - r_{03}r_{01}g_{m, BD-QFG3} \quad (9)$$

Bandwidth: The small signal equivalent circuit of the BDQFG cascode current mirror for calculating bandwidth is shown in Figure 9(a). The circuit is further simplified by assuming $C_s = C_b || (C_{sb1} + C_{sb2} + C_{sb3} + C_{sb4})$, $C_4 = C_2 || (C_{gs1} + C_{gs2} + C_{dg7})$ and presented in Figure 9(b).

The transfer function of the BDQFG cascode current mirror is given as follows: in equation 10.

From eqn. 10, the bandwidth of the BDQFG cascode current mirrors can be expressed as:

$$\omega_0 = \sqrt{\frac{g_{mBD-QFG1}g_{mBD-QFG3}}{2C_B C_S}} \quad (11)$$

Simulation

The performance of the various current mirror circuits discussed in this paper has been evaluated using PSpice software with level 7 parameters in

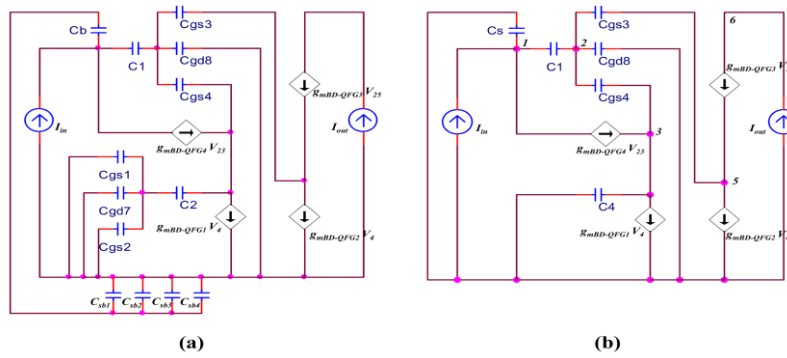


Figure 9. (a) Small signal analysis for calculating the bandwidth (b) and its equivalent circuit

$$A(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{mBD-QFG1}g_{mBD-QFG3}}{2C_B C_S \left[s^2 \left(\frac{1}{C_2} + \frac{1}{2C_B} + \frac{1}{2C_1} \right) C_2 + s \left(\frac{g_{mBD-QFG1}}{2C_2} + \frac{g_{mBD-QFG2}}{2C_2} + \frac{g_{mBD-QFG1}g_{mBD-QFG3}}{2C_B C_2} + \frac{g_{mBD-QFG1}}{2C_1} + \frac{g_{mBD-QFG3}}{2C_1} \right) \right]}$$

Equation 10

130 nm technology and utilizing a supply voltage of ± 0.5 V. The width-to-length ratios of MOSFETs M1, M2, M3, and M4 were set to $5.2 \mu\text{m} / 0.26 \mu\text{m}$, while Mp1 and Mp2 were $2.6 \mu\text{m} / 0.13 \mu\text{m}$. The capacitors C1, C2, and C3 had a capacitance of 0.1 pF. BDQFG cascode current mirror's I-V characteristics are shown in Figure 10 for input current ranging from 0 to $10 \mu\text{A}$ with increments of $2 \mu\text{A}$.

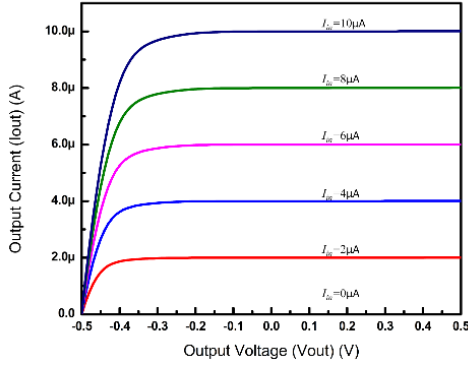


Figure 10. I-V characteristics of BDQFG MOSFET cascode current mirror

The comparative analysis of the current transfer characteristics for QFG, BD-QFG, and BDQFG cascode current mirror circuits is presented in Figure 11. As shown in Figure 11, the BDQFG cascode current mirror shows better results than the QFG and BD-QFG MOSFET current mirror circuits in terms of linearity and better current transfer ratio. The input current versus input voltage curves and percentage error ratio are presented in Figure 12 and Figure 13 respectively. Figure 14 shows the comparative output I-V characteristics of the current mirrors at an input current of $10 \mu\text{A}$. Figures 15 and 16 show the frequency dependence of input and output resistance for $I_{in} = 10 \mu\text{A}$, respectively. BDQFG cascode current mirror circuit offers an input resistance of $1.43 \text{ k}\Omega$, an output resistance of $2.16 \text{ M}\Omega$, and consumes 0.14 mW of power.

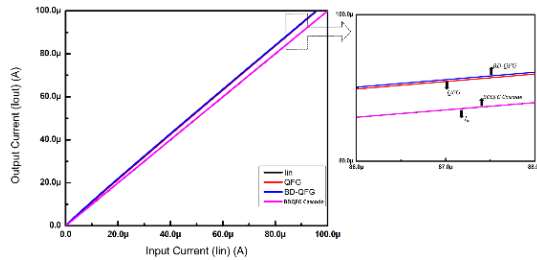


Figure 11. Comparative transfer characteristics

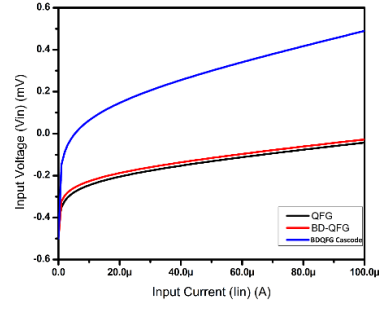


Figure 12. Comparative input voltage vs. input current characteristics

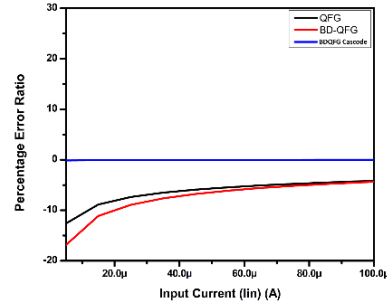


Figure 13. Current matching error ratio of QFG, BDQFG, and BDQFG cascode current mirror

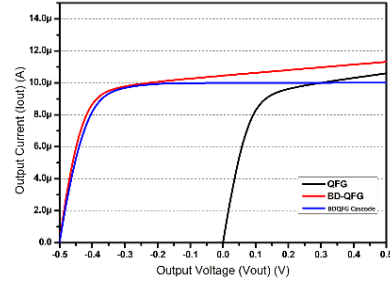


Figure 14. Current matching error ratio of QFG, BDQFG, and BDQFG cascode current mirror

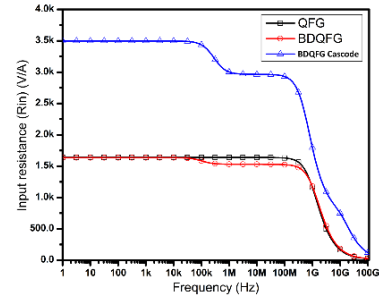


Figure 15. Input resistance vs. frequency for $I_{in} = 10 \mu\text{A}$

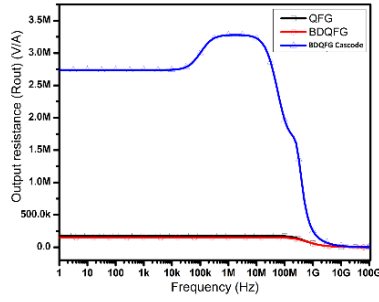


Figure 16. Output resistance vs. frequency for $I_{in} = 10 \mu A$

The comparative frequency response curves of QFG, BDQFG, and BDQFG cascode current mirror circuits are shown in Figure 17 over a frequency range of 1 Hz to 100 GHz. As evident the bandwidth of the BDQFG cascode current mirror is 664.5 MHz which is lesser than both QFG (1.08 GHz) and BDQFG current mirror circuits (1.32 GHz). Table 1 summarizes the relative performance parameters for QFG, BDQFG, and BDQFG cascode current mirror circuits.

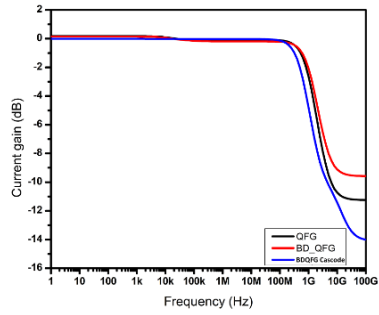


Figure 17. Comparative frequency response

Table 1. Performance comparison results of QFG, BDQFG, and BDQFG cascode current mirror circuits

Parameters	QFG CM	BD-QFG CM	BDQFG cascode CM
Power dissipation	0.10 mW	0.154 mW	0.15 mW
Input resistance	1.83 kΩ	1.63 kΩ	3.71 kΩ
Output resistance	95 kΩ	157 kΩ	2.78 MΩ
Bandwidth	1.08 GHz	1.32 GHz	664.5 MHz
Current transfer ratio	1.02	1.01	0.99

In order to improve the bandwidth of the BDQFG cascode current mirror circuit, a dc-level shifter technique is applied at the output through M5, as shown in Figure 18(a). The circuit's bandwidth is further improved by implementing a self-cascode configuration at the output side through M5 and M6 with a bias current (I_{bias}) of 100 μA , which increases the gain of the current mirror by providing additional voltage gain, resulting in further increases the bandwidth of the circuit, as

shown in Figure 18(b). The bandwidth of the BDQFG cascode employing the dc-level shifter current mirror is approximately given as:

$$\omega_0 = \sqrt{\frac{g_{mBD-QFG1} g_{mBD-QFG3}}{2C_S (C_B + C_{gs5})}} \quad (12)$$

where C_{gs5} is the gate to source voltage of M5 as shown in Figure 18(a), and bandwidth for BDQFG cascode employing self-cascode current mirror is:

$$\omega_0 = \sqrt{\frac{g_{mBD-QFG1} g_{mBD-QFG3}}{2C_S (C_B + C_{gs5} \parallel C_{gs6})}} \quad (13)$$

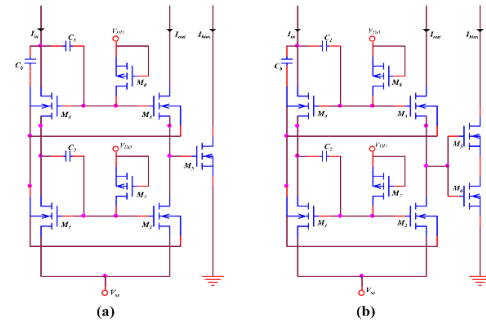


Figure 18. (a) BDQFG cascode employing dc-level shifter (b) and self-cascode current mirror circuit

On comparing Eqns. (11), (12), and (13), it can be seen that BDQFG cascode employing self-cascode current mirror circuit has higher and improved bandwidth as $C_S(C_B + C_{gs5} \parallel C_{gs6}) > C_S(C_B + C_{gs5}) > C_S C_B$. The transient response for a sinusoidal input of BDQFG cascode CM, BDQFG cascode employing dc-level shifter, and BDQFG cascode employing self-cascode CM is shown in Figure 19.

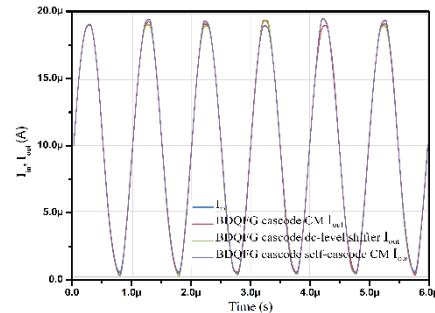


Figure 19. The transient response for a sinusoidal input of BDQFG cascode CM, BDQFG cascode employing dc-level shifter, and BDQFG cascode employing self-cascode CM

The results illustrate the output current response to a 10 kHz sinusoidal input signal with peak-to-peak amplitude of 10 μA , highlighting the circuit's transient behavior. The total harmonic distortion (THD) for each configuration is 0.90% for the BDQFG cascode, 0.91% for the BDQFG cascode with a DC-level shifter, and 0.33% for the BDQFG cascode with a self-cascode. The lower THD observed in the BDQFG cascode with a self-cascode configuration demonstrates the improved stability and linearity of the proposed circuit.

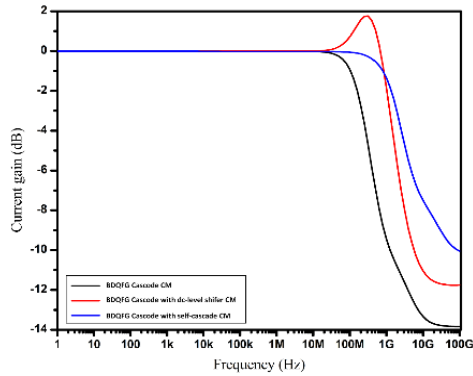


Figure 20. Frequency response of BDQFG cascode, BDQFG cascode employing dc-level shifter and self-cascode current mirror for bandwidth calculation

The comparative frequency response of BDQFG cascode, BDQFG cascode employing dc-level shifter, and self-cascode current mirror are shown in Figure 20, which clearly shows an improvement of bandwidth in BDQFG cascode

employing self-cascode current mirror compared to BDQFG cascode and BDQFG cascode employing dc-level shifter current mirror circuit. In order to investigate the nonlinearity of the presented circuits, total harmonic distortion (THD) analysis has been carried out by applying a sine wave at frequencies of 10, 50, and 100 MHz in relation to the input signal. Table 2 shows the calculated values of total harmonic distortion (THD) for the BDQFG cascode, BDQFG cascode employing dc-level shifter, and self-cascode current mirror circuits.

In order to assess the robustness of a circuit design a Monte Carlo analysis simulation technique is used in the presence of parameter variations. In this case, 100 runs of Monte Carlo analysis were performed for both AC and DC analysis of BDQFG cascode employing self-cascode current mirror circuit with a 1%, 5%, and 10% variation in the model parameter and variation in threshold voltage. For DC analysis, the maximum mean deviation value for $I_{in} = 100 \mu\text{A}$ was -90.82×10^{-09} , and the standard deviation was 3.63×10^{-06} . Similarly, the Monte Carlo yield for AC analysis revealed a mean deviation of 2.38×10^{-09} and a standard deviation of 173.79×10^{-09} for a bias current of 100 μA . Monte Carlo simulation for 100 runs of the BDQFG cascode employing self-cascode current mirror circuit for 5% model parameter and threshold variation in terms of I-V characteristics and frequency response is shown in Figures 21, 22. Figure 23 shows the temperature effect on I-V characteristics for BDQFG cascode employing a self-cascode current mirror.

Table 2. Analysis of total harmonic distortion for BDQFG cascode, BDQFG cascode employing dc-level shifter and self-cascode current mirrors

Amplitude of input signal (μA)	THD for BDQFG cascode			THD for BDQFG cascode employing dc-level shifter			THD for BDQFG cascode employing self-cascode		
	10 MHz	50 MHz	100 MHz	10 MHz	50 MHz	100 MHz	10 MHz	50 MHz	100 MHz
10	0.17	1.16	3.19	0.24	3.38	5.93	0.23	157.76	102.45
15	0.21	1.19	3.22	0.25	2.29	5.75	0.37	220.41	416.34
20	0.29	1.25	3.27	0.28	3.21	5.56	0.62	179.67	102.78
25	0.40	1.38	3.39	0.35	3.15	5.33	121.35	154.08	106.86
30	0.53	1.61	3.57	0.45	3.12	5.10	80.20	81.02	99.08
35	0.66	1.95	3.90	0.56	3.15	4.92	76.12	132.19	73.37
40	0.78	2.36	4.36	0.67	3.31	4.86	97.66	71.33	35.67
45	0.88	2.79	4.91	0.78	3.46	4.93	133.36	61.63	80.62
50	0.98	3.20	5.49	0.87	3.70	5.11	69.24	69.71	40.66
55	1.06	3.59	6.06	0.97	3.94	5.36	122.35	72.01	39.36
60	0.13	3.94	6.61	1.08	4.23	5.67	93.49	28.43	24.10
65	1.20	4.27	7.13	1.18	4.59	6.06	98.87	32.30	41.17
70	1.27	4.57	7.64	1.30	4.98	6.50	54.08	59.52	38.16
75	1.34	4.89	8.13	1.45	5.44	6.98	36.49	50.07	41.81
80	1.42	5.19	8.61	1.62	5.94	7.56	62.27	55.27	26.91
85	1.54	5.48	9.11	1.84	6.53	8.21	37.89	75.88	28.92
90	1.73	5.81	9.64	2.15	7.12	9.13	38.68	80.22	34.20
95	2.05	6.22	10.24	2.57	8.13	10.37	50.16	96.79	36.59
100	2.62	6.88	11.02	3.17	9.18	11.92	39.95	121.72	29.47

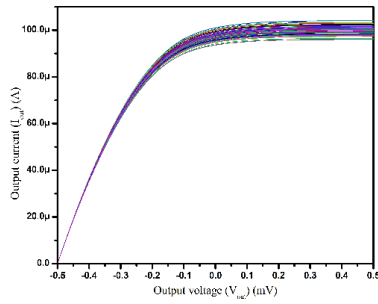


Figure 21. Monte Carlo analysis of the BDQFG cascode employing self-cascode current mirror's I-V characteristics at $I_{in} = 100 \mu A$ using a 5% model parameter and 100 runs of threshold variation

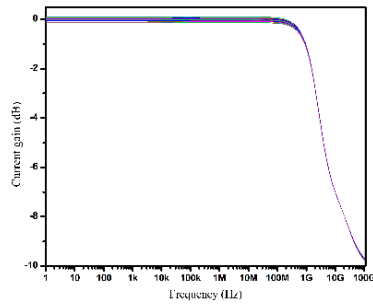


Figure 22. Monte Carlo analysis of the BDQFG cascode employing self-cascode current mirror's frequency response using a 5% model parameter and 100 runs of threshold variation

The temperature stability of the BDQFG cascode current mirror employing self-cascode configuration showing I-V characteristics across four key temperature points ($0^\circ C$, $27^\circ C$, $50^\circ C$, and $100^\circ C$) at a $10 \mu A$ input current as shown in Figure 23. The output current maintains consistency across this temperature range throughout the full -0.5V to +0.5V output voltage span.

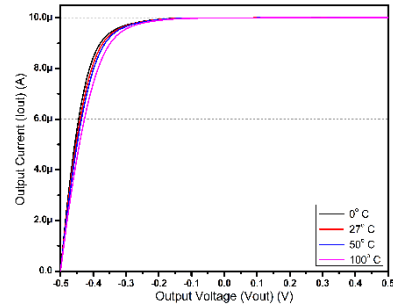


Figure 23. Temperature effects on I-V characteristics at $I_{in} = 10 \mu A$ for BDQFG cascode employing self-cascode current mirror

The circuit layout of the BDQFG cascode employing a self-cascode current mirror is shown in Figure 24. Table 3 shows the comparative simulation results of the current mirror topologies.

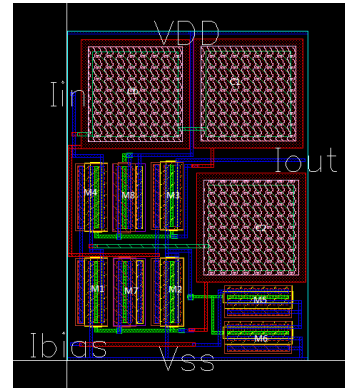


Figure 24. The layout of the proposed BDQFG cascode employing a self-cascode current mirror

Power dissipation across the different current mirror configurations, shown in Table 1 reveals that the power consumption is of 0.10 mW for QFG CM, 0.154 mW for BD-QFG CM, and 0.15 mW for

Table 3. Results of current mirror topologies comparison for low voltage operation

Parameters	BD simple CM (Blalock and Allen, 1995)	BD cascode CM (Blalock et al., 1998)	FGMOS simple CM (Ramirez et al., 1995)	FGMOS cascode CM (Aggarwal and Gupta, 2009)	BDQFG cascode employing dc-level shifter	BDQFG cascode employing self-cascode
Mirroring accuracy	No matching	Very poor	poor	Excellent	Excellent	Excellent
% Error ratio	-	-	53.3	0.84	0.10	0.10
Input resistance	350	350	9 k	13 MΩ	3.7 kΩ	3.7 kΩ
Output resistance	15 k	30 kΩ	200 kΩ	28 kΩ	2.7 MΩ	2.7 MΩ
Bandwidth	NA	NA	NA	NA	1.4 GHz	1.93 GHz
Power consumed	411.71 μW	1.3 mW	33.18 μW	25.165 μW	0.15 mW	0.15 mW

BDQFG cascode CM under $\pm 0.5V$ supply voltage. Further BDQFG cascode CM offer higher output impedance ($2.78\text{ M}\Omega$) compare to BDQFG CM ($157\text{ k}\Omega$) while sacrificing bandwidth with improved current mirroring accuracy. Moreover Table 3 shows the proposed BDQFG cascode CM employing self-cascode dissipate 0.15 mW of power with improve input, output resistance and bandwidth parameters compared with other low-voltage techniques like BD (Blalock and Allen, 1995), BD cascode (Blalock *et al.*, 1998), FGMOS (Ramirez *et al.*, 1995), and FGMOS cascode CM (Aggarwal and Gupta, 2009).

Conclusion

In this paper, a novel configuration of a current mirror employing the BDQFG cascode technique has been presented and analyzed. BDQFG cascode current mirror circuit has shown an improved current mirror accuracy and output resistance as compared to BD and BDQFG current mirror circuits. However, the cascode configuration has resulted in a reduction in bandwidth. To increase the bandwidth of the circuit, further improvements have been proposed in terms of BDQFG cascode employing a dc-level shifter and self-cascode stage at the output while keeping all other parameters same. The BDQFG cascode employing a dc-level shifter and BDQFG cascode employing self-cascode current mirror circuits have been compared with other low-voltage current mirror circuits available in the literature, and it has been found that the BDQFG cascode employing dc-level shifter and BDQFG cascode employing self-cascode current mirror circuits exhibit better performance in terms of bandwidth while maintaining improved current mirror accuracy and output resistance. Therefore, the proposed BDQFG cascode current mirror circuits may be considered as promising candidates for low-voltage, and low-power dissipating circuit application.

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