

A TRANSFORMER LESS SELF-BALANCING HIGH-GAIN 7-LEVEL INVERTER WITH MINIMUM COMPONENT COUNT AND LOWER VOLTAGE STRESSES FOR SOLAR PV APPLICATIONS

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Abstract

This article presents a revolutionary 7-level, nine-times voltage boosting property converter. The main disadvantage of traditional Multilevel Inverter (MLI) is that, in order to use renewable energy sources, a high-voltage DC-DC chopper must be tolerant of raise input voltage. The suggested converter makes use of ten switches, two inductors, four diodes, three switching capacitors, and just one DC supply. The capacitor's voltage equalizes itself automatically. Less components are needed and a capacitor is used instead of a DC source to create the switched capacitor MLI. To produce the output voltage waveforms with seven levels, the switching Inductor/capacitor must be appropriately charged and discharged. Without requiring a voltage regulating circuit with a closed loop, the suggested inverter can self-balance the capacitor's voltage. Because of the continuous series-parallel discharge and charging over a full cycle, three capacitors receive equal charges from the input source and the inductors. Compared to the majority of recently produced topologies, the suggested 7-level Switched Capacitor (SC) inverter involves a reduced number of switches, driver diodes, capacitors, also semiconductor switches. Additionally, four pairs of switches run simultaneously using the same control signal, simplifying the control system, and eight of the ten the fundamental frequency is used by switches to function. An elementary frequency switching system is employed to regulate the inverter's output. On the PSIM/MATLAB platform, the suggested structure's voltage-boosting and self-balancing capabilities are verified.

Keywords: Multilevel Inverter; PV Generation; Switched Capacitor; Switched Inductor

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Introduction

Multilevel inverters have revolutionized the power electronics industry by providing a workable solution to voltage issues in high-power applications. While high voltage has always been challenging to generate, multilevel inverters have drastically changed the traditional approach to generate boosted voltage waveforms (Nagaraju, 2023). Their use is expanding rapidly, and they are increasingly being used in the commercial and industrial sectors (Jahan *et al.*, 2018). The use of renewable energy sources is also becoming more widespread, as reducing pollution and reaching carbon neutral emissions are currently global priorities that require power converter research (Prabaharan and Palanisamy, 2017; Ismeil *et al.*, 2023). Numerous power converters, including inverters that change DC to AC and vice versa, have been the subject of research in recent years. The widespread usage of multilayer inverters (MLIs) is the last strategy to accomplish this goal (Sivapriya and Kalaiarasi, 2023). At a time when installing renewable energy systems is growing in popularity globally, multilevel inverters are essential DC to AC converters (Dhanamjayulu *et al.*, 2020a). Since renewable energy sources, such as solar power cells, ultra-capacitors, and battery backup systems, are frequently composed of several low-voltage DC sources, they are ideal for building numerous interconnected dc-links. A comparable scenario is offered by hydrogen-based fuel cells, which are being investigated for use in energy-intensive applications, such as onboard power systems (Chen *et al.* 2019). Since its initial proposal in the 1970s, inverters with multiple levels have been the focus of extensive research and development. These days, a wide range of high-power applications, including solar power, electric vehicles, and industrial drives, frequently use multilayer inverters (Addagatla and Boini, 2023). Multilevel inverter technology has established itself as a reliable and reasonably priced method of achieving excellent outcomes. Harmonic waveforms with minimal distortion. The development of multilayer inverter technology has been driven by the increasing demand for high voltage applications with low distortion (Krishnaveni and Rajender, 2024). The conventional two-level inverter was the preferred choice for low-power applications, but it has limitations when high voltage is involved. Large losses and reduced efficiency result from the dual-level inverter's production of final products with square waves and high harmonic distortion. The multilayer inverter, on the other hand, solves

this problem by producing output waveforms with minimal distortion, which results in increased efficiency and less losses. Multilevel inverters combine multiple levels of DC sources to produce the desired output voltage waveform (Panda *et al.* 2021). These topologies vary in the number of DC sources and control mechanism used (Chakraborty *et al.*, 2015). The flying capacitor inverter uses capacitors to store energy and regulate voltage levels, whereas the diode clamped inverter uses multiple diodes to clamp the output voltage. The cascaded H-bridge converter uses many H-bridge modules, each with its own DC supply, to generate the desired output waveform (Siddique *et al.*, 2019a; Hussan *et al.*, 2021).

Multilevel inverters offer several benefits over traditional 2-level inverters. Among these advantages are decreased harmonic distortion, increased efficiency, improved reliability, and less stress on the power electronics components (Nagaraju and Boini, 2025). Furthermore, improved voltage and current waveforms from multiple inverters reduce electromagnetic interference and acoustic pollution. Multilevel inverter technology has gained a lot of interest in the renewable energy sector, where high-voltage, low-distortion waveforms are crucial (Aljafari *et al.*, 2024). Multiple inverters have been shown to increase the efficiency and dependability of the power transformation process in wind, solar, and other green energy systems. Moreover, multilayer inverters have been shown to increase the effectiveness of the energy conversion mechanism in electric vehicles, increasing their range and reducing charging times (Jakkula *et al.*, 2022). The switched capacitor multilevel inverter (SCMLI), a new power electronics technique, converts several AC voltage levels from DC voltage. A series of switched capacitor cells generate its several output voltages. The capacity of an SCMLI to produce higher-quality waveforms as an output is one of its main advantages. The inverter can do this by simulating a sinusoidal waveform with a range of voltage levels. As a result, harmonic distortion is reduced, which is crucial for a variety of applications, such as motor control and renewable energy systems. Additionally, by accurately controlling the output voltage, the duty ratio for the switching signals can be altered, providing fine control over the load.

High voltage, high power, and high efficiency are all possible with MLI-produced DC-AC conversion. Smaller filter sizes, decreased harmonic content, and lower individual device ratings are

some of the features of MLIs. Previously, cascaded H-bridge architectures (CHB), neutral point clamped (NPC), and flying capacitors (FC) were used to create MLIs. Significant numbers of capacitors are used in higher level flying capacitor and neutral point clamped (NPC) topologies, which lead to issues with cost and dependability as well as the need for capacitor voltage balancing (Celanovic and Boroyevich, 2000). Since their inception, a number of altered designs have been developed to eliminate their shortcomings. The latter developed topologies outnumber the three traditional topologies in terms of components. Researchers are actively developing MLIs utilizing an application-based approach, with the goals of tolerance for errors, flexibility, efficiency, weight, and volume limitations (Kumar and Fernandes, 2017; Sarwar *et al.*, 2021). A lot of effort has been put into creating structures with fewer devices (Dewangan *et al.*, 2019; Omer *et al.*, 2020). In a similar vein, researchers have also investigated fault-tolerant reduced device count topologies (Kumar *et al.*, 2021) and device count optimization (Siddique *et al.*, 2020a). However, there are problems because many DC sources are required, which makes control difficult and impractical, especially when employing renewable energy sources with different voltage levels. First off, capacitors are initially seen in MLIs in the two conventional forms, NPC and FC. SCMLI-based topologies, which contain series/parallel configurations of capacitors and switch modules, have lately caught the attention of researchers (Samizadeh *et al.*, 2020), particularly for applications where the ability to increase voltage is advantageous.

A significant rise in low magnitude voltage, such that of fuel cells or solar systems, is made possible by this boosting function. This explains the need to do away with boost DC/DC converters, which are otherwise necessary as intermediary devices (Krishnaveni *et al.*, 2025). significantly reducing the overall generating system's size, efficacy, and complexity. Nonetheless, there are currently initiatives underway to tackle the issues brought on by the overabundance of devices. It's noteworthy to note that (Jahan *et al.*, 2018) investigates using capacitors in place of a CHB's several DC sources, requiring the use of a single DC source. The setup proposed in (Siddique *et al.*, 2019b) can generate nine levels using a single dc supply, two capacitors, nine switches, and a dual motivational element. Capacitor voltage self-balancing has the benefit of not requiring extra hardware or control electronics. Two capacitors, one dc source, and three connected H-bridge constructions may also provide seven levels with a boosting factor of three (Lee, 2018). The large

number of pieces in (Taghvaei *et al.*, 2017) could negatively impact the system's dependability. presented a seven-level enhanced Packed U-Cell active rectifier based on floating weighting factor and an artificial neural network-based model predictive control (ANN-MPC) based on Lyapunov stability. When converting DC to AC electricity, switching capacitor based multilayer inverters (SC-MLI) are becoming more and more necessary because of their exceptional performance (Roy and Sadhu, 2020). The SC MLI setup is expanded to include energy from renewable sources (RE) and better-performing electric vehicles (Panda *et al.*, 2020a). When multilayer inverters (MLI) produce a less distorted output voltage staircase pattern, the structure is more appropriate for enhancing the power quality. Although the researchers have developed numerous different types of MLIs, the three conventional designs are diode clamped MLIs (DC MLIs), cascaded H-bridge inverters (CHB MLIs), and flying capacitor MLIs (FC MLIs). Compared to 2-level inverters, these traditional MLIs offer several benefits. Nevertheless, 3-level MLIs have both similar and unique limitations. For severe industrial activities requiring particular voltage output up to eight levels, these conventional MLIs are fully employed. To generate a higher-level voltage waveform, they need a large number of devices. DC MLIs require more diodes and DC link capacitors, FC MLIs require more capacitors, and CHB MLIs require more DC power supply. As a result, several of the disadvantages of conventional MLIs are removed, including the requirement for an increase in the number, size, and cost of inverters, as well as DC sources and switches (Sandeep and Yaragatti, 2017). To solve the imbalance problem with capacitor voltage, several researchers this year focused on topological progress in MLI arrangement. Many MLIs with fewer devices have been presented in the last few years (Sivamani and Mohan, 2022). However, due to complex support algorithms, these setups are unable to self-boost. Circuits like as those in (Sivamani and Mohan, 2022), have been proposed to mitigate the imbalance problem in a capacitor's voltage. Additionally, (Babaei and Gowgani, 2013) offers a 7-level topology with the advantage of a SC MLI-based method. Furthermore, (Dhanamjayulu *et al.*, 2020b) reduces the total number of switches by using ten switches rather than twenty to generate a voltage output with seven levels. Several SC MLIs were later made public in published studies. For some of them, you need more switches, more capacitors, higher voltage stress, or low voltage gain. A new, small module structure has been developed as a result of it.

Another advantage of an SCMLI is its ability to operate at higher switching frequencies. Because the output voltage is generated using multiple levels, a higher switching frequency can be achieved without the need for higher voltage switching devices. This reduces switching losses and increases overall efficiency (Thota and Jeevananthan, 2020). Furthermore, since capacitors generate the output voltage, large inductors which can be expensive and heavy are not required. The need for careful capacitor balancing is one of the main challenges with SCMLI technology. Because each inverter cell has a different capacitor value need, it is essential to make sure that the voltage of each capacitor is balanced (Siddique *et al.*, 2022). This can be achieved using a variety of balancing techniques, such as energy redistribution and voltage clamping. To ensure that the switching signals are synced, the inverter must also be carefully designed. In this work, a novel seven-level SC MLI with just ten switches and a single DC supply is designed. This design allows a nine-time enhanced staircase to be produced from a single DC source. For MLI control, several switching techniques have recently surfaced (Hosseinazadeh *et al.*, 2020). Numerous techniques are used, such as the multi vector space methodology in (Hosseinazadeh *et al.*, 2020; Balasubramonian and Rajamani, 2014), the selective distortion reduction pulse-width modulation (SHE PWM) in (Balasubramonian and Rajamani, 2014), and (Hosseinazadeh *et al.*, 2020), which explains the usage of multiple triangular carriers in the sinusoidal switching pulse technique.

The primary benefit of the MLIs is its capacity to produce stairway pattern output. The ability of the MLIs to produce a staircase pattern output is its main advantage. As a result, the output has less harmonic content than three-level inverters. Consequently, MLIs of different types are widely used in traction, electric vehicles, photovoltaic (PV), and FACT applications (Roy *et al.*, 2021). In both symmetrical and asymmetrical modes, the modularity feature of traditional CHB MLI which has numerous applications is investigated. Asymmetrical circuits use fewer switches to produce more levels than symmetrical circuits. However, many DC sources and additional switches are needed. Because of this, it is essential to design a new inverter construction with fewer components and a single DC-bus. Even though the structures offered by (Sun *et al.*, 2016; Jahan *et al.*, 2018) made an effort to minimize the number of switches, a significant reduction was not achieved. In (Roy *et al.*, 2021), the conventional setup incorporates an additional charging circuit. One advantage is that the output voltage can be increased using just one input source. In (Sun *et al.*, 2016), an alternative

circuit to the conventional CHB MLI was also modified. The operation makes it clear that the capacitors are being filled and drained as necessary, which contributes to the increase in output voltage. The ideas proposed in applications (Barzegarkhoo *et al.*, 2022) are particularly interesting for PV applications. One of the circuits reduces the number of sources by utilizing a self-balancing capacitor based on the energy regulating concept, while the other MLI uses the switched-capacitor (SC) concept to balance the voltage. The former is incapable of significantly raising voltage, but the other MLI can. Newly proposed SC topologies consider a reduction in the number of parts and the stress on each switch to generate boost output voltage (Lee *et al.*, 2019; Panda *et al.*, 2020b). Because it generates a high-gain output without requiring a huge transformer or inductor, this architecture can be employed in a variety of applications while maintaining the intrinsic voltage balancing of each capacitor. For capacitor voltage balancing, certain circuit topologies are mentioned in (Choi and Kang, 2014) that need to be taken into account. minimizing the number of switches used. Many different seven-level configurations that consider both single-stage and voltage boosting applications have been suggested. To reduce the leakage current, topologies with NPC and common-neutral connections have been suggested more recently. All additional benefits are retained for the former categories, which are suggested in (Chen *et al.*, 2021), while the latter are added in (Krishnaveni and Rajender 2025). Another challenge with SCMLI technology is its complex control circuitry. The inverter requires a complex control circuit since the switching signals and capacitor voltages need to be properly regulated. This can be challenging to design and implement, particularly for high-power applications. Despite these challenges, SCMLI technology has many intriguing applications. One potential use is for renewable energy systems to communicate with the grid, which requires high-quality AC waveforms. Additionally, SCMLI technology is used in motor control, where exact control over the output voltage is essential. Compared to conventional two-level inverters, they have a number of benefits (Siddique *et al.*, 2019c). However, because it necessitates precise capacitor balance and complex control circuitry, the technique is challenging to design and implement. Despite these challenges, there are many promising potentials for SCMLI technology, particularly in motor control, alternative energy sources, and practical applications. Because of this, researchers are now concentrating on the switched capacitor multilayer (Ye *et al.*, 2019). When everything is taken into account, the Selective Harmonic

Elimination-Pulse Width Modulation (SHE-PWM) control approach is great; it eliminates output voltage harmonics and is based on a low switching frequency. The SHE PWM control method is used in this study to control the inverter's switching angles and output voltage. Applications utilizing sustainable and renewable energy sources were scaling up low input-side DC voltages is required are suitable for the recommended inverter. The PSIM/MATLAB software is used to simulate and assess the suggested converter capability.

Operation of Proposed 7-L SI/SC Multi-Level Inverter

The suggested 7-Level switched inductive and switched capacitor (SI-SC) based multi-level inverter topology comprises ten power switches (S1 to S10), two inductors (L1 and L2), three capacitors (C1, C2, and C3), and four diodes (D1, D2, D3, and D4). The input voltage source V_{in} serves as the inverter's input, and V_o serves as its output voltage. The Figure 1 shows single DC source 7-L SI-SC MLI, a multilayer inverter based on switched inductor and switched capacitor, operates in single phase. This circuit has advantages of identical pulse triggering for the different switches. Switches S1 and S2 are triggered identically. And switches S7 and S8 triggered at a time. And also Switches S4, S9 triggered along with S5, S10.

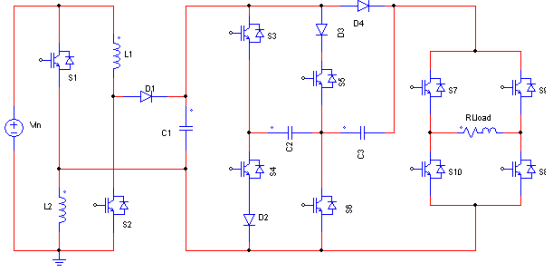


Figure 1. 7-Level SI/SC based seven level converters

Operating modes of 7-Level SI/SC based MLI.

Ten switches and two capacitors are used to create the output voltage of a seven-level staircase waveform. At the resultant voltage waveform, there are three positive and three negative levels and one zero level make up the seven levels. $\pm 3V_{in}$, $\pm 6V_{in}$, $\pm 9V_{in}$, and 0 are produced by the structure using input voltage source V_{in} . The operational analysis is provided, taking into consideration the inductive load and the fact that all of the switches are made of antiparallel diodes. The following thirteen operating modes are available to generate the seven levels of the output waveform:

Mode I (Level_1 ($3V_{in}$), high frequency power switches S1 and S2 are kept off).

In this operating mode, the output level $+3V_{in}$ is obtained when switches S1, S2, S3, S4, S5, S9, and S10 are in turn off mode and S6, S7 and S8 are in turn on mode. Diode D1 and D4 is in forward conduction, D2 and D3 are reverse blocking mode, the capacitors C1 and C3 are charged by input power source V_{in} , inductors L1 and L2. The stored energy in Inductors is at a level of input voltage. capacitor C2 is in ideal mode. The output level $+3V_{in}$ is achieved by the series combination of V_{in} , VL1 and VL2. the direction of charging and discharging currents are shown in Figure 2. Green arrows represent the charging current path of capacitor C1, red arrows represent the charging current path of capacitor C3 and blue arrows represents the load current supply path by V_{in} inductors L1 and L2.

$$V_{out} = V_{in} + V_{L1} + V_{L2} \quad (1)$$

In previous mode L1 and L2 are charged to supply voltage. Substituting that in equation (1) we get,

$$V_{out} = V_{in} + V_{in} + V_{in} = 3V_{in} \quad (2)$$

Similarly, the capacitor C3 voltage is

$$V_{C3} = 3V_{in} \quad (3)$$

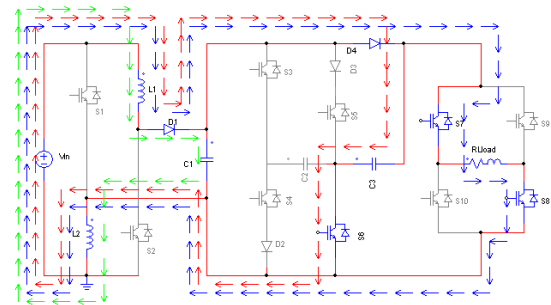


Figure 2. Mode I (Level_1) Direction of charging and discharging currents

Mode II (Level_1 ($3V_{in}$), high frequency power switches S1 and S2 are kept on).

In this mode, the output level $+3V_{in}$ is obtained when switches S3, S4, S5, S9, and S10 are in turn off mode, S1, S2, S6, S7, and S8 are in turn on mode. Diode D4 is in forward conduction mode, D1, D2 and D3 are reverse blocking mode, the capacitors C1 and C3 will supply its stored energy at a level of $+3V_{in}$ to the load. The input voltage source V_{in} is going to power both inductors L1 and L2. the direction of both recharging and draining currents are shown in Figure 3. Green arrows represent the charging current path of inductor L2

and charging current path of inductor L1 represents by blue arrow in left side loop, red arrows represent the discharging current path of capacitor C3 and blue arrows in right side loop represents the load current supply path by capacitor C1.

Therefore, the output voltage is equal to capacitor C3 voltage, i.e.

$$V_{out} = V_{C3} = 3V_{in} \quad (4)$$

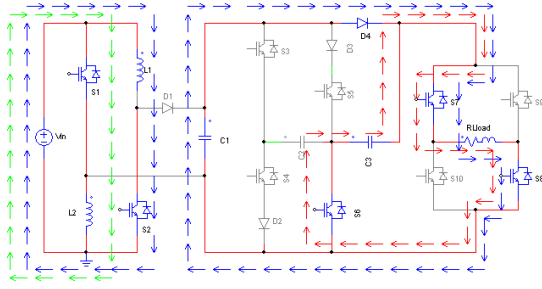


Figure 3. Mode II (Level_1) Direction of charging and discharging currents

Mode III (Level_2 (6Vin), high frequency power switches S1 and S2 are kept off).

In this operating mode, the level two output voltage +6Vin is obtained when switches S1, S2, S3, S6, S9, and S10 are in turn off mode and S4, S5, S7, and S8 are in turn on mode. Diode D1, D2 and D3 is in forward conduction, D4 is reverse blocking mode, The input voltage source Vin energizes the capacitors C1 as well as C2, inductors L1 and L2. The stored energy in Inductors is at a level of input voltage. capacitor C3 is in discharging mode its voltage is at a level of 3Vin which is charge in mode II. the output voltage +6Vin is achieved by the series combination of Vin, VL1, VL2 and VC3. the direction of charging and discharging currents are shown in Figure 4. Green arrows represent the charging current path of capacitor C1, red arrows represent the charging current path of capacitor C2 and blue arrows represents the load current supply path by Vin, inductor L1, inductor L2 and capacitor C3.

The output voltage is,

$$V_{out} = V_{in} + V_{L1} + V_{L2} + V_{C3} \quad (5)$$

substituting equation (2) and (3) in equation (5) we get,

$$V_{out} = 3V_{in} + 3V_{in} = 6V_{in} \quad (6)$$

Capacitor C1 voltage is,

$$V_{C1} = V_{in} + V_{L1} + V_{L2} = 3V_{in} \quad (7)$$

Similarly, Capacitor C2 voltage is,

$$V_{C2} = V_{in} + V_{L1} + V_{L2} = 3V_{in} \quad (8)$$

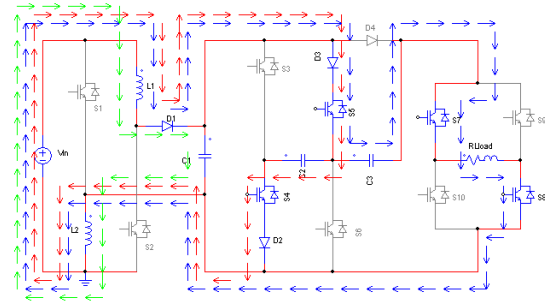


Figure 4. Mode III (Level_2) Direction of charging and discharging currents

Mode IV (Level_2 (6Vin), high frequency power switches S1 and S2 are kept on).

In this mode, the output level +6Vin is obtained when switches S3, S6, S9, and S10 are in turn off mode, S1, S2, S4, S5, S7, and S8 are in turn on mode. Diode D1 and D4 is in reverse biased mode, D2 and D3 are in forward conduction mode, the capacitors C1, C2 and C3 will supply the stored energy at a level of +6Vin to the load. Capacitors all are at a voltage level of +3Vin but capacitors C1 and C2 are in parallel and C3 is in series with the combination. The input voltage source Vin will charge both inductors L1 and L2. The direction of charging and discharging currents are shown in Figure 5. Green arrows represent the charging current path of inductor L2 and charging current path of inductor L1 represents by blue arrow in left side loop, red arrows represent the discharging current path of capacitor C2 and blue arrows in right side loop represents the load current supply path by capacitor C1 and C3.

The output voltage in this mode is,

$$V_{out} = V_{C1} + V_{C3} \quad (9)$$

Substituting equation (4) and (7) in equation (9) we get

$$V_{out} = 3V_{in} + 3V_{in} = 6V_{in} \quad (10)$$

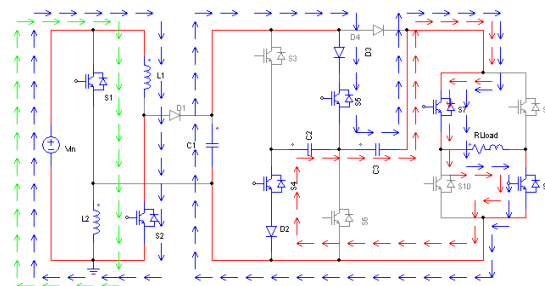


Figure 5. Mode IV (Level_2) Direction of charging and discharging currents

Mode V (Level_3 (9Vin), high frequency power switches S1 and S2 are kept off).

In this operating mode, the level three output voltage +9Vin is achieved when switches S1, S2, S4, S5, S6, S9, and S10 are in turn off mode and S3, S7, and S8 are in turn on mode. Diode D1 is in forward conduction mode, diodes D2, D3, and D4 are in reverse blocking mode, the capacitors C1 is charged by its input source Vin, inductors L1 and L2. The stored energy in Inductors is at a level of input voltage. Capacitors C2 and C3 is in discharging mode its voltage is at a level of 3Vin which is charge in mode III and Mode II. The output voltage +9Vin is achieved by the series combination of Vin, VL1, VL2, VC2 and VC3. The direction of charging and discharging currents are shown in Figure 6. Green arrows represent the charging current path of capacitor C1, and blue arrows represents the load current supply path by supplied by supply voltage, L1, L2, C2 & C3.

The output voltage is,

$$V_{out} = V_{in} + V_{L1} + V_{L2} + V_{C2} + V_{C3} \quad (11)$$

Substituting equation (2), (4) and (8) in equation (11) we get

$$V_{out} = 3V_{in} + 3V_{in} + 3V_{in} = 9V_{in} \quad (12)$$

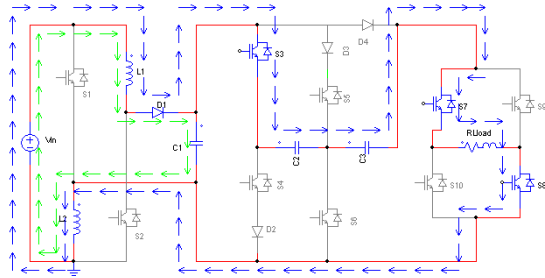


Figure 6. Mode V (Level_3) Direction of charging and discharging currents

Mode VI (Level_3 (9Vin), high frequency power switches S1 and S2 are kept off).

In this mode, the level three output voltage +9Vin is obtained when switches S4, S5, S6, S9, and S10 are in turn off mode, S1, S2, S3, S7, and S8 are in turn on mode. Diode D1, D2, D3 and D4 is in reverse biased mode, the capacitors C1, C2 and C3 will supply the stored energy at a level of +9Vin to the load. Capacitors all are at a voltage level of +3Vin which is stored in previous modes but capacitors C1, C2 and C3 are in series. Vin will charge the inductors L1 and L2. The direction of charging and discharging currents are shown in Figure 7. Green arrows represent the charging

current path of inductor L2 and charging current path of inductor L1 represents by blue arrow in left side loop, and blue arrows in right side loop represents the load current supply path by capacitor C1, C2 and C3.

The output voltage is,

$$V_{out} = V_{C1} + V_{C2} + V_{C3} \quad (13)$$

Substituting equation (3), (7) and (8) in equation (13) we get

$$V_{out} = 3V_{in} + 3V_{in} + 3V_{in} = 9V_{in} \quad (14)$$

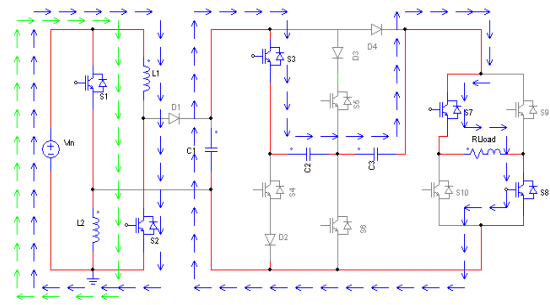


Figure 7. Mode VI (Level_3) Direction of charging and discharging currents

Mode VII (Level_-1 (-3Vin), high frequency power switches S1 and S2 are kept off).

This mode is identical to the mode I, but the status of the switches S7, S8, S9, S10 are changed. During this operating mode, the output level -3Vin is achieved when switches S1, S2, S3, S4, S5, S7, and S8 are in turn off mode and S6, S9, and S10 are in turn on mode. Diode D1 and D4 is in forward conduction, D2 and D3 are reverse blocking mode. Capacitors C1 and C3 are charged by Vin, inductors L1 and L2. The stored energy in Inductors is at a level of input voltage, capacitor C2 is in ideal mode. The output level -3Vin is achieved by the series combination of Vin, VL1 and VL2. The direction of charging and discharging currents are shown in Figure 8. Green arrows represent the charging current path of capacitor C1, red arrows represent the charging current path of capacitor C3 and blue arrows represents the load current supply path by inductors L1, L2 and supply voltage.

$$V_{out} = -V_{in} - V_{L1} - V_{L2} \quad (15)$$

In previous mode L1 and L2 are charged to supply voltage. Substituting that in equation (1) we get,

$$V_{out} = -V_{in} - V_{in} - V_{in} = -3V_{in} \quad (16)$$

Similarly, the capacitor C3 voltage is

$$V_{C3} = 3V_{in} \quad (17)$$

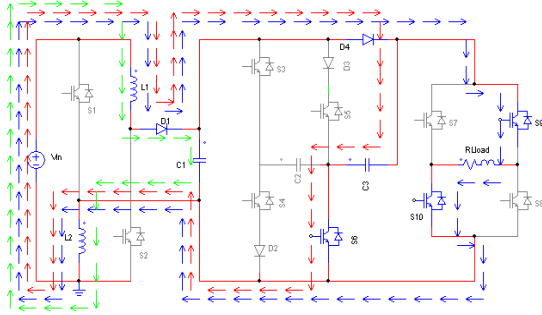


Figure 8. Mode VII (Level_-1) Direction of charging and discharging currents

Mode VIII (Level_-1 (-3V_{in}), high frequency power switches S1 and S2 are kept on).

This mode is identical to the mode II, but the status of the switches S7, S8, S9, S10 are changed. In this mode, the output level -3V_{in} is obtained when switches S3, S4, S5, S7, and S8 are in turn off mode, S1, S2, S6, S9, and S10 are in turn on mode. Diode D4 is in forward conduction mode, D1, D2 and D3 are reverse blocking mode, the capacitors C1 and C3 will supply the stored energy at a level of -3V_{in} to the load. The V_{in} will charge both inductors L1 and L2. the direction of charging and discharging currents are shown in Figure 9. Green arrows represent the charging current path of inductor L2 and charging current path of inductor L1 represents by blue arrow in left side loop, red arrows represent the discharging current path of capacitor C3 and blue arrows in right side loop represents the load current supply path by capacitor C1.

Therefore, the output voltage is equal and opposite to capacitor C3 voltage,

$$\text{i.e } V_{out} = -V_{C3} = -3V_{in} \quad (18)$$

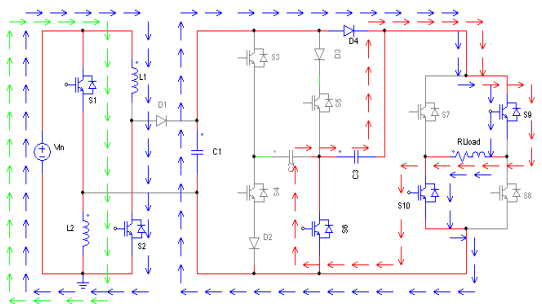


Figure 9. Mode VIII (Level_-1) Direction of charging and discharging currents

Mode IX (Level_-2 (-6V_{in}), high frequency power switches S1 and S2 are kept off).

This mode is identical to the mode III, but the status of the switches S7, S8, S9, S10 are changed,

in this operating mode, the output level -6V_{in} is obtained when switches S1, S2, S3, S6, S7, and S8 are in turn off mode and S4, S5, S9, and S10 are in turn on mode. Diode D1, D2 and D3 is in forward conduction, D4 is reverse biased mode, The source voltage V_{in} charges both capacitors C1 and C2. Inductors L1 and L2. The stored energy in Inductors is at a level of input voltage, capacitor C3 is in discharging mode its voltage is at a level of 3V_{in} which is charge in mode II. the output voltage -6V_{in} is achieved by the series combination of V_{in}, V_{L1}, V_{L2} and V_{C3}. The direction of charging and discharging currents are shown in Figure 10. Green arrows represent the charging current path of capacitor C1, red arrows represent the charging current path of capacitor C2 and blue arrows represents the load current supply path by inductors L1, L2, supply voltage and capacitor C3.

The output voltage is,

$$V_{out} = -V_{in} - V_{L1} - V_{L2} - V_{C3} \quad (19)$$

substituting equation (16) and (17) in equation (19) we get

$$V_{out} = -3V_{in} - 3V_{in} = -6V_{in} \quad (20)$$

Capacitor C1 voltage is

$$V_{C1} = V_{in} + V_{L1} + V_{L2} = 3V_{in} \quad (21)$$

Similarly, Capacitor C2 voltage is

$$V_{C2} = V_{in} + V_{L1} + V_{L2} = 3V_{in} \quad (22)$$

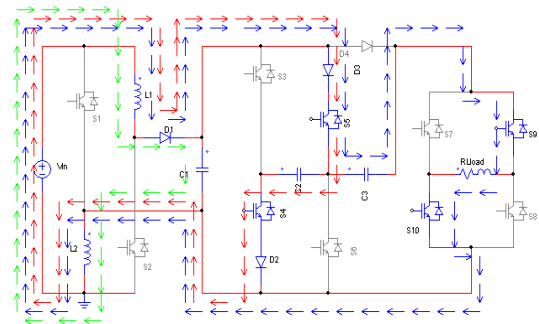


Figure 10. Mode IX (Level_-2) Direction of charging and discharging currents

Mode X (Level_-2 (-6V_{in}), high frequency power switches S1 and S2 are kept on).

This mode is identical to the mode IV, but the status of the switches S7, S8, S9, S10 are changed. In this mode, the output level -6V_{in} is obtained when switches S3, S6, S7, and S8 are in turn off mode, S1, S2, S4, S5, S9, and S10 are in turn on mode. Diode D1 and D4 is in reverse biased mode,

D2 and D3 are in forward conduction mode, the capacitors C1, C2 and C3 will supply the stored energy at a level of $-6V_{in}$ to the load. Capacitors all are at a voltage level of $-3V_{in}$ but capacitors C1 and C2 are in parallel and C3 is in series with the combination. Both inductors L1 and L2 will be charged by the input voltage source V_{in} . The direction of charging and discharging currents are shown in Figure 11. Green arrows represent the charging current path of inductor L2 and charging current path of inductor L1 represents by blue arrow in left side loop, red arrows represent the discharging current path of capacitors C2 & C3 and blue arrows in right side loop represents the load current supply path by capacitor C1.

The output voltage in this mode is

$$V_{out} = -V_{C1} - V_{C3} \quad (23)$$

Substituting equation (18) and (21) in equation (23) we get

$$V_{out} = -3V_{in} - 3V_{in} = -6V_{in} \quad (24)$$

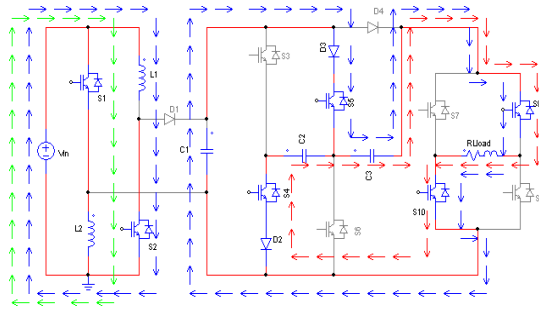


Figure 11. Mode X (Level_-2) Direction of charging and discharging currents

Mode XI (Level_-3 (-9Vin), high frequency power switches S1 and S2 are kept off).

This mode is identical to the mode V, but the status of the switches S7, S8, S9, S10 are changed. In this operating mode, the output level $-9V_{in}$ is obtained when switches S1, S2, S4, S5, S6, S7, and S8 are in turn off mode and S3, S9, and S10 are in turn on mode. Diode D1 is in forward conduction mode, diodes D2, D3, and D4 are in reverse blocking mode, the capacitors C1 is charged by V_{in} , inductors L1 and L2. The stored energy in Inductors is at a level of input voltage. Capacitors C2 and C3 is in discharging mode its voltage is at a level of $3V_{in}$ which is charge in mode III and Mode II. The output voltage $-9V_{in}$ is obtained by the series combination of V_{in} , V_{L1} , V_{L2} , V_{C2} and V_{C3} . The direction of charging and discharging currents are shown in Figure 12. Green arrows represent the

charging current path of capacitor C1, and blue arrows represents the load current supply path by supplied by supply voltage, L1, L2, C2 & C3.

The output voltage is,

$$V_{out} = -V_{in} - V_{L1} - V_{L2} - V_{C2} - V_{C3} \quad (25)$$

Substituting equation (16), (18) and (22) in equation (25) we get

$$V_{out} = -3V_{in} - 3V_{in} - 3V_{in} = -9V_{in} \quad (26)$$

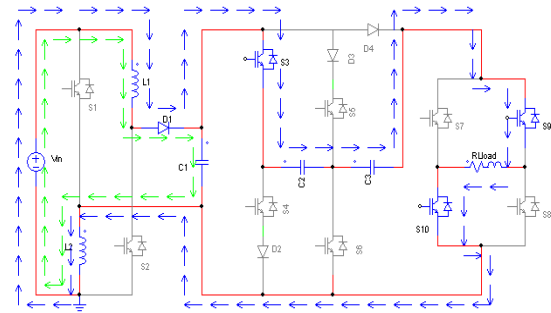


Figure 12. Mode XI (Level_-3) Direction of charging and discharging currents

Mode XII (Level_-3 (-9Vin), high frequency power switches S1 and S2 are kept on).

This mode is identical to the mode VI, but the status of the switches S7, S8, S9, S10 are changed. In this mode, the output level $-9V_{in}$ is achieved when switches S4, S5, S6, S7, and S8 are in turn off mode, S1, S2, S3, S9, and S10 are in turn on mode. Diode D1, D2, D3 and D4 is in reverse biased mode, the capacitors C1, C2 and C3 will supply the stored energy at a level of $-9V_{in}$ to the load. Capacitors all are at a voltage level of $-3V_{in}$ which is stored in previous modes but capacitors C1, C2 and C3 are in series. Both inductors L1 and L2 are magnetized by the input voltage source V_{in} . The direction of charging and discharging currents are shown in Figure 13. Green arrows represent the charging current path of inductor L2 and charging current path of inductor L1 represents by blue arrow in left side loop and blue arrows in right side loop represents the load current supply path supplied by capacitors C1, C2 & C3.

The output voltage is,

$$V_{out} = -V_{C1} - V_{C2} - V_{C3} \quad (27)$$

Substituting equation (17), (21) and (22) in equation (27) we get

$$V_{out} = 3V_{in} + 3V_{in} + 3V_{in} = 9V_{in} \quad (28)$$

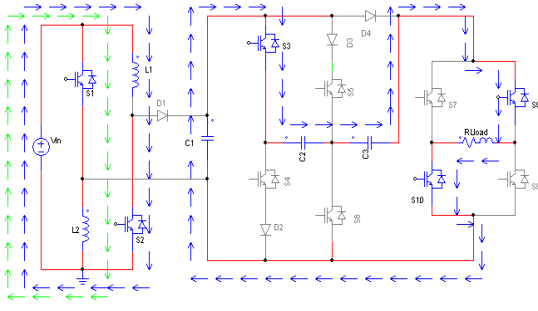


Figure 13. Mode XII (Level_-3) Direction of charging and discharging currents

Mode XIII (Level_0 (0Vin))

In this configuration, the two remaining S7 and S9, are in conduction mode and switches S1, S2, S3, S4, S5, S6, S8, and S10 are in the off position. The zero-level output can be produced by activating either two lower switches or two top switches connected to the bridge circuit. Table 1 displays the switching scheme of the 7-L SI/SC MLI with seven distinct voltage levels (+Vin, -Vin, +2Vin, -2Vin, +3Vin, -3Vin, and 0Vin) as well as the capacitors and inductors charging and discharging status i.e represented by arrows, upward arrow stands for charging and downward arrow represents discharging status.

Voltage Self-balancing Analysis

It is evident based on the functional analysis covered in Section 2.1, whereby the capacitor C1 gets charged both when the power is switched on and off. Capacitor C2 discharged in the remaining states after being charged between +6Vin and -6Vin volts. Conversely, the capacitor C3 experiences charging at Vin and -Vin, and discharging at 6Vin and -6Vin. As a result, the recharging and draining

process is balanced. Additionally, the capacitors are discharged to the source to the load and charged in parallel with the DC source. Notable features include the minimal parasitic resistance and sufficient charging and discharging time for each capacitor in a single basic cycle. As a result, during the operation of the circuit, the voltage across Naturally, the capacitor is kept at Vin. This confirms the self-balancing nature, and the right capacitance is selected with the least amount of voltage ripple possible while accounting for the greatest time to discharge.

The presence of DC voltage Vdc suggests that we are dealing with a modulated system, likely a PWM inverter or rectifier. In such systems, the AC-side quantities are often related to the DC-link voltage Vdc through a modulation factor. A proportionality constant k_Ψ is introduced, which is often related to modulation index or control gain, giving:

$$C_n \geq L_1 \frac{\Delta Q_c}{\Delta V_c} = \frac{2I_{op} \cos(\theta_n) \cos(\Phi)}{k_\Psi V_{dc}} \quad (29)$$

where C_n is constant or coefficient related to the system. L_1 is another constant or coefficient. $\frac{\Delta Q_c}{\Delta V_c}$ could represent capacitor's amount of discharge rate. (Q_c) with respect to capacitor's ripple voltage (V_c). I_{op} could represent an operational current or a reference current. θ_n and Φ are angles, possibly related to phase shifts in alternating current systems. k_Ψ might be a constant, possibly linked to a system parameter. V_{dc} is the DC voltage. This equation likely describes the dynamic behavior of a capacitor in a power electronics circuit. It is particularly useful in DC-link capacitor sizing for inverters, where charge variations depend on AC current components and modulation strategies.

Table 1. 7-Level SI/SC MLI's switching states along with the periods for capacitor/Inductor charging/discharging status, upward arrow represents charging status and downward arrows represents discharging status

Voltage Level	Conducting switches	Inductor L1 and L2	Capacitor C1	Capacitor C2	Capacitor C3
0	S7, S9 S8, S10	- -	- -	- -	- -
+3Vin	S6, S7, S8 S1, S2, S6, S7, S8	↓ ↑	↑ ↓	- -	↑ ↓
+6Vin	S4, S5, S7, S8 S1, S2, S4, S5, S7, S8	↓ ↑	↑ ↓	↑ ↓	↓ ↓
+9Vin	S3, S7, S8 S1, S2, S3, S7, S8	↓ ↑	↑ ↓	↓ ↓	↓ ↓
-3Vin	S6, S9, S10 S1, S2, S6, S9, S10	↓ ↑	↑ ↓	- -	↑ ↓
-6Vin	S4, S5, S9, S10 S1, S2, S4, S5, S9, S10	↓ ↑	↑ ↓	↑ ↓	↓ ↓
-9Vin	S3, S9, S10 S1, S2, S3, S9, S10	↓ ↑	↑ ↓	↓ ↓	↓ ↓

Pulse width modulation

The generation of staircase voltage waveforms is the aim of MLIs with low turn on and off intervals. It is possible to select each switching function's order in order to reduce THD. This is known as "pulse width modulation" (PWM) with "selective harmonic elimination" (SHE). Additionally, there are high-frequency modulation approaches that, although they result in a lower THD, trade off with higher switching losses. "Space vector modulation and sinusoidal pulse width modulation" (SPWM) with triangle carriers are two instances of high-frequency modulation techniques. SHE PWM has the benefit of a lower switching frequency. Then SHE PWM is frequently used in large power inverters, where Switching losses could be extremely significant. With the best possible selection of switching functions, certain harmonics in the output voltage are eliminated as the switching frequency increases, permitting the inverter to run at a waveform with a lesser switching frequency. The transcendental equations are also calculated to determine the switching angles using the Newton-Raphson approach and the resultant theory technique. The former method only provides a small number of solutions sets and necessitates a good initial prediction. This paper explains how to use the SHE PWM technique to determine the optimal switching angle value for a 7-L SI/SC MLI. Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) is a technique used in power electronics to control the output voltage of inverters while eliminating specific lower-order harmonics. The key objective of SHEPWM is to determine the optimal switching angles ($\theta_1, \theta_2, \dots, \theta_n$) that satisfy certain voltage and harmonic elimination criteria.

Steps to Determine the Optimal Switching Angles in SHEPWM

Formulation of Fourier Series Expansion:

The output voltage waveform of an inverter is represented as a Fourier series.

The general form of the output voltage $V(t)$ is:

$$V(t) = \sum_{n=1,3,5,\dots}^{\infty} V_n \sin(n\omega t) \quad (30)$$

The fundamental component and harmonic components are determined from this expansion.

Mathematical Formulation of SHEPWM Equations:

The harmonic components of the output voltage can be expressed as:

$$V_n = \frac{4V_{dc}}{\pi} \sum_{k=1}^n \cos(n\theta_k) \quad (31)$$

For an N-level inverter with "n" switching angles, the set of nonlinear transcendental equations is:

- for specific harmonics to be eliminated

$$\sum_{k=1}^n \cos(n\theta_k) = 0, \quad (32)$$

- to control fundamental voltage

$$\sum_{k=1}^n \cos(n\theta_k) = M, \quad (33)$$

Here, M is the modulation index.

Solving Nonlinear Equations:

The system of nonlinear transcendental equations is solved to determine the switching angles ($\theta_1, \theta_2, \dots, \theta_n$)

Common numerical methods used for solving these equations include:

- **Newton-Raphson Method:** Iterative approach that refines the values of angles.
- **Genetic Algorithms (GA):** Optimization-based technique used when equations are highly nonlinear.
- **Particle Swarm Optimization (PSO):** AI-based optimization technique for better convergence.

Constraints on Switching Angles:

The switching angles must satisfy: $0 < \theta_1 < \theta_2 < \dots < \theta_n < \pi/2$ This ensures proper switching sequence and avoids overlap.

Verification and Implementation:

- Once the optimal angles are determined, they are used in the inverter's pulse generation scheme.
- Harmonic spectrum analysis (using FFT) is performed to verify harmonic elimination and fundamental voltage control.

MATLAB Script for SHE-PWM Output Waveform

```

-----
clc;
clear;
close all;

%% Parameters
N = 3; % Number of switching angles
M = 0.8; % Modulation index (0 to 1)
Vdc = 1; % DC Bus voltage (normalized)
Harmonics = [5, 7, 11]; % Harmonics to eliminate

%% Initial Guess for Switching Angles
theta0 = linspace(10, 80, N)' * pi / 180; % Initial angles in radians

%% Solve SHE Equations Using Newton-Raphson

```

```

F = @(theta) SHE_Equations(theta, M,
Harmonics);
options = optimoptions('fsolve', 'Display',
'iter', 'TolFun', 1e-6);
theta_sol = fsolve(F, theta0, options);
theta_sol_deg = theta_sol * 180 / pi; %
Convert to degrees

%% Display Results
disp('Optimized Switching Angles
(Degrees):');
disp(theta_sol_deg);

%% Generate SHE-PWM Output Waveform
T = linspace(0, 2*pi, 1000); % Time samples
Vout = zeros(size(T)); % Initialize output
voltage

for i = 1:length(T)
    t = T(i);
    for j = 1:N
        if mod(t, 2*pi) < theta_sol(j)
            Vout(i) = Vdc;
        elseif mod(t, 2*pi) < pi
            Vout(i) = -Vdc;
        end
    end
end

%% Plot Output Waveform
figure;
plot(T * 180/pi, Vout, 'b', 'LineWidth',
2);
grid on;
xlabel('Time (Degrees)');
ylabel('Inverter Output Voltage (V)');
title('SHE-PWM Stepped Output Waveform');
xlim([0 360]);
ylim([-Vdc-0.1 Vdc+0.1]);

%% FFT Analysis (Harmonic Spectrum)
Fs = length(T) / (2*pi); % Sampling
frequency
Y = fft(Vout); % Compute FFT
L = length(Y);
P2 = abs(Y/L); % Two-sided spectrum
P1 = P2(1:L/2+1); % Single-sided spectrum
P1(2:end-1) = 2*P1(2:end-1);

f = Fs*(0:(L/2))/L; % Frequency axis

figure;
stem(f, P1, 'r', 'LineWidth', 1.5);
grid on;
xlabel('Harmonic Order');
ylabel('Magnitude');
title('Harmonic Spectrum of SHE-PWM
Output');

%% Function to Define SHE Equations
function F = SHE_Equations(theta, M,
Harmonics)
    N = length(theta);
    F = zeros(N,1);

    % Fundamental Harmonic
    F(1) = sum(cos(theta)) - M * (pi / 4);

    % Eliminate Selected Harmonics
    for k = 1:length(Harmonics)
        h = Harmonics(k);
        F(k+1) = sum(cos(h * theta));

```

```

end
end
output of the SHE PWM Optimized Switching
Angles (Degrees)Using Newton-Raphson
:    9.4645,    37.8152,    88.2090
-----

```

Based on the above switching angles control pulses are given for switches. Figure 14 Explains about control signals for switches. When switches S7, S8 are turn on we will get positive levels and when S9, S10 are turn on we will get negative voltage level. In figure blue color signal is for level₁ (3Vin) & level₋₁ (-3Vin) and it is given for Switch S6. Red color signal is for level₂ (6Vin) & level₋₂ (-6Vin) and it is given for Switch S4 and S5. Yellow color signal is for level₃ (9Vin) & level₋₃ (-9Vin) and it is given for Switch S3.

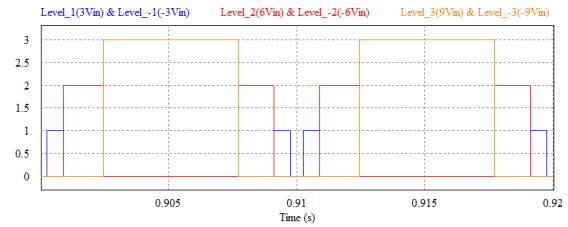


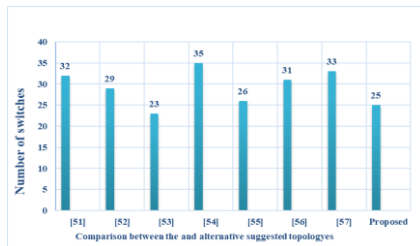
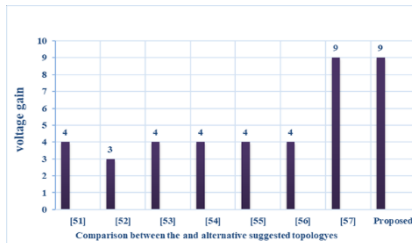
Figure 14. Control Signals for Switches for different levels

Comparative Estimation

A comparison with a few chosen topologies has shown the developed boost inverter topology's comparison capabilities. Table 2 shows a contrast between the recommended 7-level 9 times voltage gain boost inverter design and some of the other topologies that have been proposed previously. The number of switches, diodes, inductors, capacitors, input sources, gate drivers, gains in the topology, and whether or not polarity is created intrinsically are the factors that are compared. In (Barzegarkhoo *et al.*, 2021), the architecture uses more gate drivers and an additional capacitor but has one fewer switch than the recommended topology. The recommended topology is lower than the TSV and MBV. There is the same quantity of components overall in (Dhara and Somasekhar, 2021)'s topology, but it has a low voltage gain of three and a large TSV. The topology in (Iqbal *et al.*, 2020 and Siddique, *et al.*, 2020b) has a larger MBV and a larger voltage rating capacitor. The topology in (Wang *et al.*, 2021) is more extensive in terms of switches used and has a higher TSV value than the suggested topology. In contrast to the recommended topology, H-bridge is used in Reference (Jakkula *et al.*, 2022) to generate polarity, which results in high TSV and MBV values.

Table 2. A comparison of the proposed topology with other seven-level topologies

Converter proposed in	No. of switches	No. of inductors	No. of capacitors	No. of diodes	No. of gate drivers	Voltage gain	Maximum blocking voltage	H-bridge	Total no. of components
(Barzegarkhoo <i>et al.</i> , 2021)	14	0	4	0	14	4	4	No	32
(Dhara and Somasekhar, 2021)	12	0	4	2	11	3	3	Yes	29
(Iqbal <i>et al.</i> , 2020)	10	0	2	1	10	4	4	No	23
(Siddique, <i>et al.</i> , 2020b)	16	0	3	0	16	4	4	No	35
(Wang <i>et al.</i> , 2021)	10	0	3	3	10	4	4	Yes	26
(Jakkula <i>et al.</i> , 2022)	15	0	3	0	13	4	3	No	31
(Nagaraju and Rajender, 2023)	8	2	5	12	6	9	9	Yes	33
Proposed	10	2	3	4	6	9	3	Yes	25

**Figure 15. comparison of suggested configuration based on the quantity of switches****Figure 16. comparison of suggested configuration based on the voltage gain**

The recommended generalized topology and many rival generalized topologies are contrasted in Table 2. That have been proposed recently. The suggested design has lower TSV and MBV than the other topologies in Table 2, indicating that the switches are under less voltage stress. Its total number of components is equal to or less than that of the other items in Table 2. Comparing the topology presented here to the other topologies listed in the Table 2 below, there are more capacitors and diodes in it. The topology presented in (Nagaraju and Rajender, 2023) has high gain but a greater number of components. Figure 15, comparison of suggested configuration based on the

quantity of switches and Figure 16, comparison of suggested configuration based on the voltage-gain.

Simulation Results

IGBT switches, inductors, capacitors, and diodes make up the 7-Level SI/SC MLI, as depicted in Figure 17, and they are all simulated using the PSIM/MATLAB/Simulink platform. The simulation uses V_{in} 24V, inductors L1, L2 are rated at 100 μ H, and C1, C2, and C3 are rated at 2200 μ F. Figure 18(a) displays the output AC power supply voltage with 24V input DC voltage, Figure 18(b) shows the load current under the 500W load condition. Figure 18(c-e) are the capacitors C1, C2 and C3 balanced voltages of the suggested design under an RL load of 100 ohm - 120mH. Three balanced capacitor voltages and seven stages of output voltage with a peak amplitude of 216V are present. From Figure 19 it was observed the the suggested 7-Level SI/SC based MLI, had total harmonic distortions of 12.44%, and in the output waveform the selected harmonics of dominant 5th, 7th and 11th harmonics are eliminated. The suggested MLI's dynamic operational capability is shown in Figure 20. Figure 20(a) illustrates how the load current gradually transitions from being solely resistive to sinusoidal-like with inductive loading when the load suddenly changes. The results confirm that there are also very little ripples in the capacitor voltage. The smooth transition between the output and capacitor voltages caused by the abrupt shift in input voltage is shown in Figure 20(b). Under any scenario of operation, the capacitor voltages have been adjusted to the proper value.

During the capacitor charging process, large current spikes, also known as inrush current, are an inevitable serious problem in SC circuits. The issue is raised in every SC MLI that has been released thus far. However, a recently designed structure in (Barzegarkhoo *et al.*, 2021), overcomes the problem

of capacitor current by using a quasi-resonant cell in the input side. The quasi-resonant cell restricts the inrush current of the capacitor during charging by choosing the appropriate values for the tiny inductor and capacitor (L_{in} and C_{in}). Although the current spikes cannot be totally eliminated by the suggested

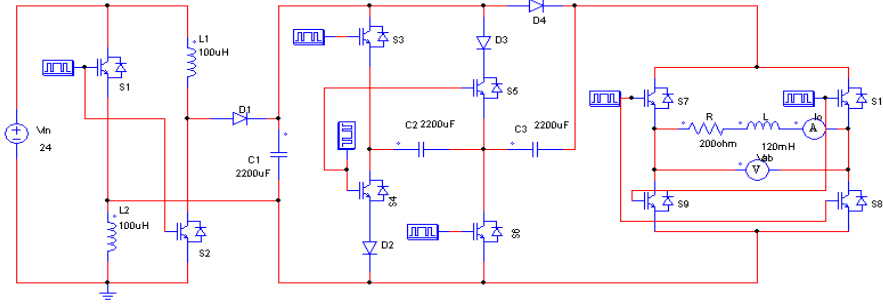


Figure 17. Simulation circuit of proposed inverter

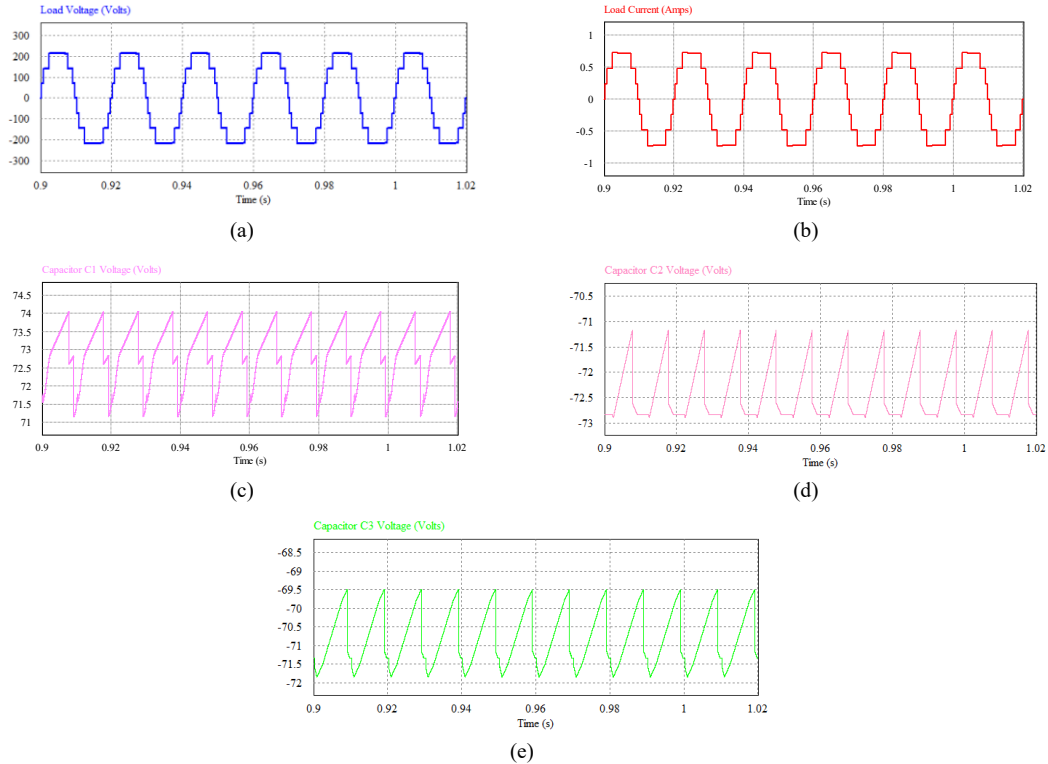


Figure 18. (a) Load voltage 18 (b) Load current 18(c-e) voltage balancing of capacitor C1, C2 and C3

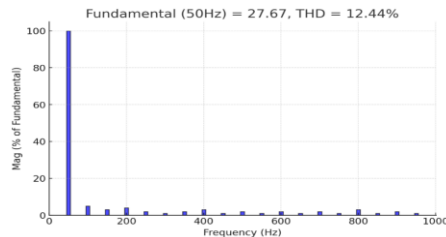


Figure 19. Total harmonic distortion of output voltage

topology as described in the article, by joining the quasi-resonant cell as in (Dhara and Somasekhar, 2021), they can be reduced. When considering the charging loop utilizing the equivalent capacitance (C_{eq}), the equivalent series resistance (R_{eq}) is taken into account. When choosing the resonant cell inductance, as follows:

$$L_{in} \geq \frac{R_{eq}^2 C_{eq}}{4} \quad (34)$$

Figure 20(c) Dynamic functioning of the suggested MLI capacitor currents in the absence of a resonant cell and Figure 20(d) Using the resonant cell, the suggested MLI capacitor currents operate dynamically. The capacitor currents as well as output voltage are depicted in Figures 20(c) and 20(d), respectively, both without and with the quasi-resonant cell used. Even after accounting for the charging path's parasitic resistance, it is evident that the charging currents of the SC type MLIs during normal operation are rather large (50 times). The

capacitor current is significantly decreased while maintaining the MLI's 7-L functionality when the resonant cell is taken into consideration.

Conclusion

For small-scale photovoltaic applications, this research suggests nine times boost seven-level inverter and a high gain generalized MLI. Low stress across the switches and capacitor self-balancing voltage are two of its benefits. A comparison analysis is carried out with current literature. The suggested architecture is appropriate for all types of loads and has been tested under various load, supply voltage, and frequency fluctuations. Additionally, the capacitor's voltage ripples stay within permitted bounds with various load fluctuations. There is a single DC source and lesser number of switches needed for the proposed 7-L SC MLI structure. Due to their self-balancing nature, the capacitors provide an output.

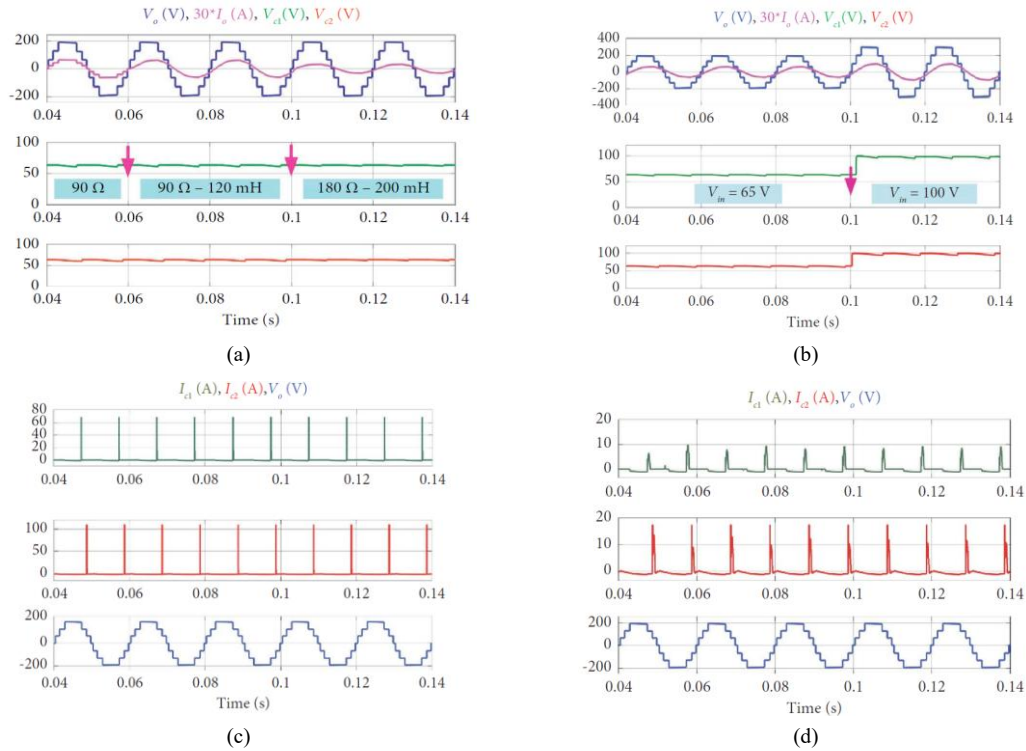


Figure 20. (a) Dynamic functioning of the suggested MLI outcome during abrupt changes in loading, (b) The suggested MLI operates dynamically in response to abrupt changes in input voltage, (c) Dynamic functioning of the suggested MLI capacitor currents in the absence of a resonant cell and (d) Using the resonant cell, the suggested MLI capacitor currents operate dynamically

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