

INVESTIGATING DOUBLE GATE LITHIUM NIOBATE-BASED METAL FERROELECTRIC METAL INSULATOR SEMICONDUCTOR (MFMIS) NCFETS THROUGH ANALYTICAL MODELING AND SIMULATION

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Abstract

As the miniaturization of silicon circuits continues, the primary challenge has shifted towards reducing energy consumption. The Boltzmann limit, a fundamental barrier in traditional semiconductor devices, has prompted the exploration of novel solutions. One promising candidate is the Negative Capacitance Field Effect Transistor (NCFET). NCFETs introduce a second insulating ferroelectric material to create a negative capacitance (CFE) effect, which counteracts the positive capacitances inherent in Field Effect Transistors (FETs). This interaction allows for lower operating voltages and enhanced energy efficiency. Silicon, a ubiquitous material in semiconductor devices, remains a focal point of this research due to its widespread use and well-understood properties. Extensive analytical studies have been conducted on silicon-based devices, examining their performance at ever-decreasing nanoscale gate levels. This work presents a significant advancement with the introduction of high-performance LiNbO₃-based NCFETs. Compared to traditional single-gate designs, the proposed LiNbO₃-based NCFET demonstrates superior performance metrics. Notably, it exhibits hysteresis-free characteristics, leading to a more stable and efficient operational region. The absence of hysteresis not only simplifies the device's operation but also enhances its reliability and scalability for future applications. In conclusion, the implementation of LiNbO₃-based NCFETs represents a promising step towards overcoming the limitations imposed by the Boltzmann limit, offering a pathway to more energy-efficient silicon circuits as they continue to shrink in size.

Keywords: Ferroelectric materials; Lithium Niobate; L-K theory; MFMIS architecture; NCFET; Silicon Circuit

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Introduction

Carbon Nanotubes (CNTs) are cylindrical nanostructures composed of carbon atoms arranged in a hexagonal lattice, offering extraordinary electrical, mechanical, and thermal properties. Due to their high conductivity, electron mobility, and flexibility, CNTs have been widely explored in nanotechnology, particularly in Field Effect Transistors (FETs) as channels for electron transport. In recent developments, researchers are moving toward lithium niobate (LiNbO_3) ferroelectric material for use in NCFETs due to its strong ferroelectric properties, such as high remnant polarization and low coercive field, which aid in reducing power consumption and overcoming the subthreshold swing limit in FETs. The integration of CNTs into NCFETs provides enhanced performance, such as improved switching speed, reduced leakage currents, and better scalability, while utilizing the negative capacitance effect of LiNbO_3 to further boost energy efficiency in nanoscale transistors. Scalability parameters of FETs have exceeded the Boltzmann tyranny limit FETs because transistors cannot control the heat produced (Horowitz *et al.*, 2005). It was suggested that the negative capacitance (NC) of capacitors composed of ferroelectric materials may be used to reduce the power dissipation of semiconductor technology below these fundamental bounds (Salahuddin and Datta (2008). FETs with ferroelectric surfaces that have negative capacitance have attracted much attention from scientists (Kobayashi, 2018; Tu *et al.*, 2018; Alam *et al.*, 2019; Bacharach *et al.*, 2019; Hoffmann *et al.*, 2019; 2021; Íñiguez *et al.*, 2019; Cao and Banerjee 2020; Khosla and Sharma, 2021; Mikolajick *et al.*, 2021).

A theoretical study has been conducted on the functioning of NCFETs (Xiao *et al.*, 2012; Jiang *et al.*, 2015) through (Chen *et al.*, 2011). However, earlier investigations into the workings of NCFETs had certain limitations. The results of earlier investigations into device performance were acquired using either an analytical technique (Sallese and Meyer, 2004; Jimenez *et al.*, 2010) or numerical simulations (Yeung *et al.*, 2013; Jain and Alam, 2014) to examine the device performance. Furthermore, because short-channel and quantum mechanical phenomena are not taken into account, the methodologies that have been provided are invalid in nodes of advanced technology. These effects alter the electrostatic profile and charge distribution along the channel. Charge dispersion, which also affects capacitance matching conditions, directly impacts MOS capacitance, which is described as the series combination of oxide and

silicon capacitances. The averaging of electrostatic forces in metallic intermediary layers explains 2-D electrostatic impacts that are anticipated to be strong in small devices (Rusu *et al.*, 2010). We can utilize a 1-D Landau design to depict ferroelectric dielectric since this intermediary metallic film creates a continuous electrostatic field inside the ferroelectric stage. In addition, we propose and study a practical design approach to optimize the enhancement of non-hysteretic functioning of NCFETs (Yeung *et al.*, 2012). We discovered that the NC greatly raises the overdrive voltage and improves the subthreshold slope (SS).

One of the most popular and important semiconductor materials in use today is silicon. Devices based on silicon account for a significant portion of semiconductor development. Some analytical studies have been done on low-dimension silicon-based devices at the nanoscale (Anvarifard and Orouji, 2015; Anvarifard, 2019). Due to its inability to scale down devices at high frequencies, silicon material poses a danger to the microelectronics revolution. Silicon has attracted a lot of current research because it is one of the well-known and traditional components for semiconductor devices (Sridevi *et al.*, 2021; 2022). A lot of analytical studies have been conducted on silicon-based technology. At low nanoscale gate levels, they have also been used (Kumar and Pravin, 2021).

The benefits of both mathematical along with analytical methods were combined in this work using an analytical model. Through numerical solutions of Landau-Khalatnikov (LK) and Poisson formulas, surface potential can be ascertained early. The formula for continuity from analytical current-voltage models can be used to calculate drain current easily. In the last stage, the system is tested with mathematical modelling, and drain current vs. gate voltage curves show a remarkable level of alignment (Lee *et al.*, 2017).

Figure 1 depicts the doping profile of the double gate structure. As a result, it is now possible to mimic FE in nanoscale devices using a one-dimensional Landau model. Because device simulators like Silvaco TCAD were unable to directly validate or construct the MFMIS architecture, the baseline technique was employed in this work. To obtain variables like charge density but also surface potential, a bulk MOSFET is simulated using Silvaco's ATLAS simulator as the starting point.

Ferroelectric NC transistors with metal-ferroelectric-metal-insulators-semiconductor (MFMIS)

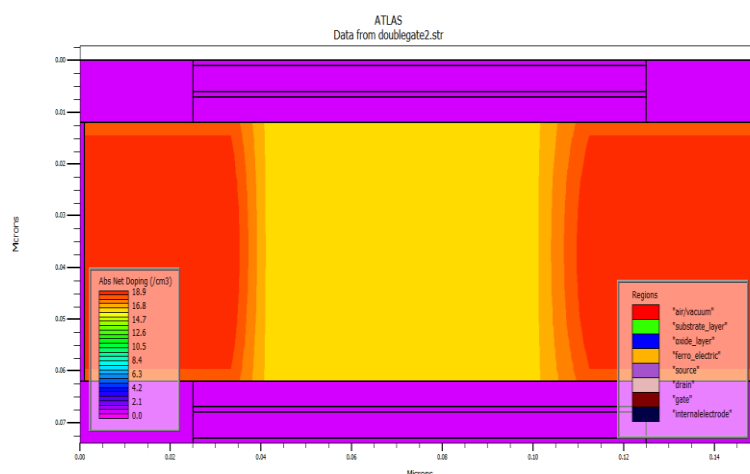


Figure 1. Doping profile of double gate structure

design are unreproducible even with the most sophisticated device simulators. Because of the intermediary level, the device can be viewed as a series combination of a normal MOSFET and an FE capacitor without the need for any boundary restrictions. The present research uses the Silvaco Atlas commercial simulator and L-K theory of ferroelectrics to compute the device performance of an MFMIS architecture (Salvatore *et al.*, 2008; Starkov and Starkov, 2014). The contribution of this study lies in the analysis and implementation of LiNbO₃-based NCFET. Key contributions include:

- The study integrates a novel structure (MFMIS-NCFET) comprising a gate electrode, SiO₂ dielectric, internal electrodes, and LiNbO₃ ferroelectric material. LiNbO₃ is chosen for its superior ferroelectric properties, which enable reduced power consumption and enhanced device performance.
- Detailed simulations using Silvaco ATLAS TCAD and MATLAB are conducted to characterize the I-V and C-V properties of the proposed NCFET. The ferroelectric 1-D Landau-Khalatnikov equation describes the dynamic polarization behaviour of LiNbO₃, offering insights into device performance under varying operating conditions.
- The negative capacitance effect facilitates lower operating voltages, leading to significant reductions in energy consumption compared to conventional FETs. Enhanced metrics such as higher ION/IOFF ratios and improved subthreshold behaviour are projected, demonstrating the potential for superior overall performance.

In summary, the present study advances comprehension and utilization of LiNbO₃-based NCFETs, providing a viable route towards developing high-performance and energy-efficient

semiconductor devices. This work is organized as follows: section 2 provides an overview of previous research, section 3 provides an overview of the L-K formula, and section 4 provides a detailed explanation of the proposed method. The planned research results and conclusion are presented in Sections 4 and 5, respectively, and the references are included in Section 6.

Literature Survey

Saritha *et al.* (2023) present a new mathematical modelling method for analyzing a ferroelectric-based NCFET to address non-uniformity in polarization switching and subthreshold behaviour. It evaluates the I-V and C-V properties of a LiNbO₃ ferroelectric material-based NCFET, considering variables like materials, gate bias modification, and thickness. Numerical simulations are performed using the Silvaco ATLAS TCAD tool, and MATLAB simulation is used to solve the ferroelectric 1-D Landau-Khalatnikov equation. The device also exhibits hysteresis behaviour at low ferroelectric thicknesses.

A comparative analysis of the performance of NCFET with single-gate, double-gate, tri-gate (FinFET), and gate-all-around (GAA) device architectures using TCAD simulations is suggested by Sakib *et al.* (2019). The electrical characteristics of these devices were simulated using aluminium-doped hafnium oxide as the FE. The results showed improved sub-threshold performance and a higher ION/IOFF ratio than baseline devices. The study also demonstrated capacitance matching between FE and MOS capacitances for non-hysteretic operation in NC-FinFET and NC-GAAFET.

This allows for maximum NC effect. The results from TCAD simulations could provide insights into the design, operation, and performance improvement of next-generation NCFET devices.

Jung (2023) studied drain-induced barrier lowering (DIBL) in an NCFET using a gate structure like an MFMIS for a junctionless double gate (JLDG) FET. They found that NC FETs exhibit negative DIBL characteristics based on the ferroelectric thickness. They used the second derivative method to understand the cause of negative DIBL, using 2D potential distribution and drain current-gate voltage curve. They also presented an analytical DIBL model for easy observation of NC FET DIBL. The results were similar to the second derivative method and were in agreement with TCAD. The negative DIBL phenomenon was found to be caused by the change in drain voltage of the charge in the ferroelectric material.

Semwal and Kranti (2023) developed analytical expressions to assess the scalability of cylindrical (CYL) nanowire and planar double gate (DG) MFMIS negative capacitance NC transistors. The results showed that at lower FE thickness, the CYL architecture outperforms planar DG NCFET due to electrostatic integrity. However, for thicker TFE, the performance of MFMIS NCFET is strongly governed by FE coupling, indicating comparable performance between DG and CYL MFMIS NCFETs. The formalism demonstrates a pragmatic design criterion for achieving sub-60 mV dec-1 subthreshold swing and DIBL-free characteristics in MFMIS NC transistors.

The study by Park *et al.* (2023) confirms that the NC effect in ferroelectric-dielectric capacitors with a metal interlayer does not appear in the metal-ferroelectric-dielectric-metal structure, contradicting the multidomain-1D Landau-Ginzburg-Devonshire model. The advanced inhomogeneous stray-field energy model fully explains the suppression of the NC effect, making an NCFET with a metal interlayer impractical.

The studies present advancements in mathematical modelling and simulation of ferroelectric-based NCFET, focusing on non-uniformity in polarization switching, subthreshold behaviour, and device architecture performance. They explore the use of different ferroelectric materials, gate bias modifications, and device thicknesses to evaluate I-V and C-V properties and hysteresis behaviour. Comparative analyses show improved sub-threshold performance and higher ION/IOFF ratios with aluminium-doped hafnium oxide as the ferroelectric material. The study also explores drain-induced barrier lowering (DIBL) characteristics and the scalability of cylindrical

nanowires and planar double gate MFMIS NCFETs. The findings offer insights into the design, operation, and performance optimization of next-generation NCFET devices.

Brief Overview of L-K Formula

The L-K formula predicts that the ferroelectric layer's Gibbs free energy density (U) can increase polarization (P) powers close to a phase transition.

$$\begin{aligned} U &= \alpha t_f P^2 + \beta t_f P^4 + \gamma t_f P^6 - V_f P \\ U &= \alpha t_f Q^2 + \beta t_f Q^4 + \gamma t_f Q^6 - V_f Q \end{aligned} \quad (1)$$

Where Q is the electrical charge of the ferroelectric element, t_f is the thickness of the ferroelectric film, V_f is the applied voltage across the ferroelectric layer, and α , β , and γ are material-dependent constants (Landau parameters). Finding the minimum of U, where we have, allows us to establish the equilibrium state of the ferroelectric layer.

$$\frac{\partial U}{\partial Q} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 - V_f = 0 \quad (2)$$

The $Q - V_f$ one can obtain a ferroelectric layer connection as

$$V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 \quad (3)$$

Considering the presented structure, (3) equation can be written as

$$V_{gate} - V_{gate(eff)} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 \quad (4)$$

where $V_{gate(eff)}$ is intermediate contact potential, and V_{gate} is applied gate voltage. Equation (4)'s left side depicts a voltage drop across ferroelectric film, while the right side illustrates the charge characteristic of FE.

The MFMIS design can be thought of as a series combination of a conventional MOSFET with a FE capacitor. The 2-D electrostatics for MOSFET were simulated using a commercial simulator named Silvaco TCAD, which also included a quantum mechanical approach, traditional Shockley-Reed-Hall recombination, drift-diffusion layout, then non-local route band-to-band design. The device's regular MOS analysis can be modelled autonomously without imposing any boundary restrictions because of the metallic intermediary stage that exists among ferroelectric

and linear dielectrics. The ferroelectric film can also be described by the 1-D Landau technique since the potential of this intermediate level is constant at all grid points. To mimic NCFET, 2-D hybrid electrostatics for MOSFET and 1-D Landau designs are solved self-consistently.

PZT is employed as a gate ferroelectric due to its various benefits, the most notable among them being its nanosecond polarization reversal and substantial dielectric constant. It is also dependable. It also has an acceptable polarization value, even in thin layers (Li *et al.*, 2004). PZT is used, however, not only because of its technological advantages but also because of its durable qualities with regard to the variation in film thickness. The layer thickness mostly affects how the ferroelectric characteristics change (Chandra and Littlewood, 2007). The next section explains the proposed work in detail.

Proposed Method and Techniques

In this study, the electrostatic field within the ferroelectric (Fe) layer of the proposed MFMS-NCFET is solved in a self-consistent manner. The device structure, depicted in Figure 2, includes a gate electrode, SiO₂ dielectric material, internal electrodes, and LiNbO₃ ferroelectric material, and source and drain contacts. The gate electrode controls the channel current through applied voltage, while the SiO₂ dielectric layer separates the gate from the internal electrodes, establishing the necessary electric field for the negative capacitance effect. LiNbO₃, selected for its exceptional ferroelectric properties, significantly reduces power consumption and enhances device performance. Source and drain contacts provide the necessary electrical connections for current flow.

The electrostatic field in the ferroelectric layer is analyzed using a self-consistent approach, with the potential distribution iteratively solved until convergence. Material properties of LiNbO₃, including its dielectric constant, polarization characteristics, and hysteresis behaviour, are incorporated into the model. Detailed I-V and C-V characteristics are simulated using the Silvaco ATLAS TCAD tool, and MATLAB is employed to solve the ferroelectric 1-D Landau–Khalatnikov equation, describing the dynamic behaviour of ferroelectric polarization. The proposed LiNbO₃-based NCFET is expected to exhibit hysteresis-free characteristics, simplifying device operation and enhancing reliability. The negative capacitance effect allows for lower operating voltages, significantly reducing energy consumption compared to traditional FETs. Superior performance

metrics, such as higher ION/IOFF ratios and improved subthreshold behaviour, are anticipated due to the unique properties of LiNbO₃.

The field's expansion abruptly stopped after a period of success, which prompted the creation of an improved method for potential constant static negative capacitance. This work provides a basic tool for NC's formation in ferroelectrics, demonstrating that the NC is inescapably generated by establishing polarization domains. In accordance with the domain layout, a workable design for a stable and reversible NCFET is shown. The operating voltage may be decreased beyond the MOSFET by utilizing negative capacitance impact in MOSFETs. Niobium, lithium, and oxygen combine to form lithium niobate. It is symmetrically reversed and possesses ferroelectricity.

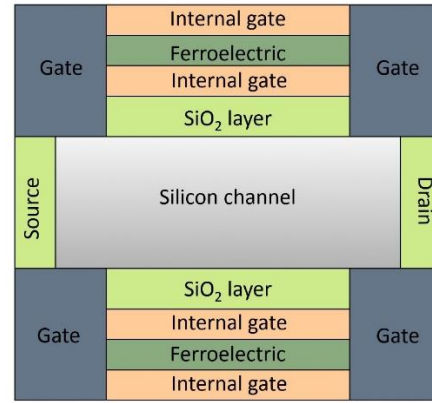


Figure 2. Illustration of the proposed structure using the diagram

We compute the gate charge of double-gate FinFET ($Q_{G, mos}$) that is, an internal-gate charge of NC-FinFET for every internal-gate voltage ($V_{G, mos}$) using (Shen *et al.*, (2015) to get the inversion capacitance (C_{inv}). One can ascertain C_{inv} by,

$$C_{inv} = \frac{dQ_{G, mos}}{dV_{G, mos}} \quad (5)$$

One can estimate inversion charge (Q_{inv}) for NCFET by taking into account 1D steady-state L-K formula for voltage drop across ferroelectric layers.

$$V_{FE} = \frac{3\sqrt{3}}{2} T_{FE} E_c \left[-\frac{Q_{G, mos}}{P_r} + \left(\frac{Q_{G, mos}}{P_r} \right)^3 \right] \quad (6)$$

Where T_{FE} , E_c , and P_r stand for ferroelectric thickness, coercive field, and remnant polarization, accordingly. The internal gate charge, $Q_{G, mos}$, is considered to be roughly equivalent to polarization within the ferroelectric component in this equation.

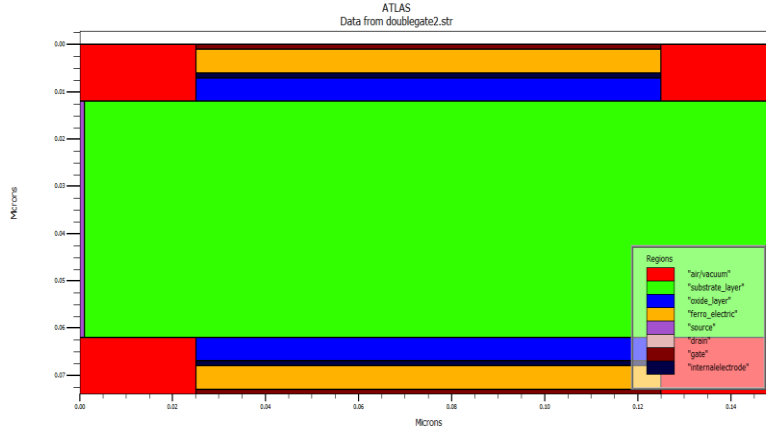


Figure 3. Regions of the double gate structure

Equation $V_{G, mos}$ may be used to compute voltage across ferroelectric, or V_{FE} , given a $Q_{G, mos}$. As a result, NCFET's matching gate voltage may be found:

$$V_G = V_{G, mos} + V_{FE} \quad (7)$$

From equation (6), the ferroelectric negative capacitance ($C_{FE} = dQ_{G, mos} + V_{FE}$) can be derived as

$$\frac{1}{C_{FE}} = \frac{3\sqrt{3}}{2} T_{FE} E_C \left[-\frac{1}{P_r} + \frac{3Q_{G, mos}^2}{P_r^3} \right] \quad (8)$$

Under strong inversion, internal-gate charge $Q_{G, mos}$ is roughly equivalent to inversion charge (Q_{inv}). As a result, NC-FinFET's quantum Q_{inv} structure could be built.

We linked the 1D steady-state L-K formula (formula 6) with TCAD simulation to derive TCAD numerical properties of the NC-FinFETs. In the process, TCAD simulation that self-consistently solves coupled Poisson-Schrodinger formulas was used to retrieve inversion charge density at every bias point of baseline FinFET. Formula (7) may then be used to determine V_{FE} corresponding to every bias and NC-FinFET's inversion charge properties.

The NC-FinFET's internal voltage amplification, or A_V , may be written as

$$A_V = \frac{\partial V_{G, mos}}{\partial V_G} = \frac{|C_{FE}|}{|C_{FE}| - C_{inv}} \quad (9)$$

Larger A_V might be produced since $|C_{FE}|$ is close to C_{inv} , according to formula (9). For everyone, T_{FE} is optimized in this study while being constrained by a non-hysteresis procedure. The results and discussion of the proposed methodology are presented in the section that follows.

Result and Discussion

The analysis of various features and a large number of experimental results are used to validate the proposed approach. The device is simulated using the Silvaco ATLAS TCAD tool for a detailed analysis of its I-V and C-V characteristics. MATLAB is employed to solve the ferroelectric 1-D Landau-Khalatnikov equation, which describes the dynamic behaviour of the ferroelectric polarization.

Figure 3 shows the regions of the double gate structure for the proposed method using Silvaco TCAD simulation. the layers in this study have the following thicknesses: the substrate layer, which is 50 nm thick and green in the figure, the oxide layers, which are 5 nm thick, the ferroelectric layer, which is 5 nm thick, the source and drain electrodes, which are 50 nm thick as well as violet and pink in the figure, and finally the gate and internal electrodes, which are 1 nm thick with brown and dark-blue in the figure. Substrate is 1×10^{16} in the doping profile, followed by 1×10^{19} for the source and drain.

The dual gate structure for the technique is depicted in Figure 4. In this diagram, the silicon materials are indicated by orange, while the vacuum materials are shown by yellow. In the diagram, SiO_2 is blue, and the conductor for the proposed method is shown in violet. The polarization finding has been validated using the proposed approach. Transverse Wave oscillations' geometrical direction is described by a property called polarisation (Chaudhary and Sahu (2020)). The polarization to electric field/voltage graph of the ferroelectric material has a negative slope, indicating negative capacitance (Sajad *et al.*, 2021). Using the LK formula (Equation 6) depicted in Figure 3, the hypothetical construction of the LiNbO_3 ferroelectric material is projected.

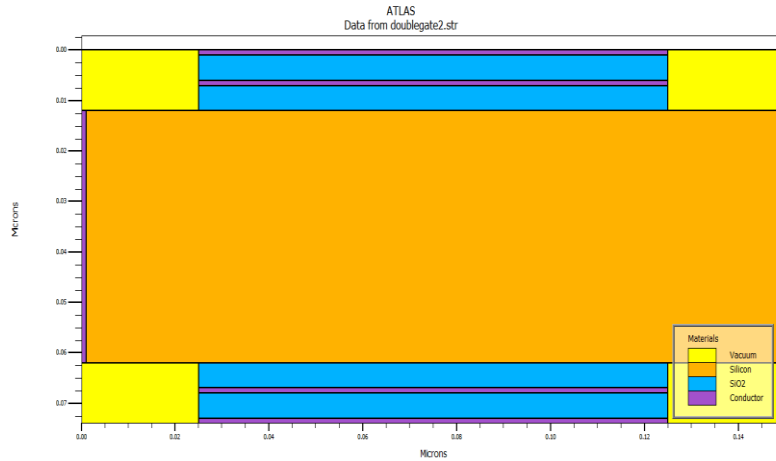


Figure 4. Double Gate structure

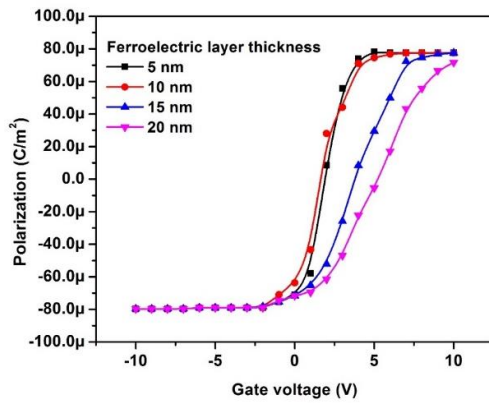


Figure 5. Polarization with double gate structure

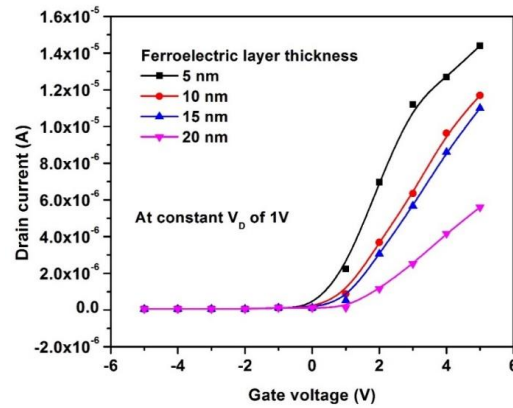
Figure 6. I-V Characteristics of double gate structure with varying thickness of LiNbO₃

Figure 5 illustrates the polarization behaviour of a double gate structure with varying thicknesses of LiNbO₃ layers. When an external gate voltage is applied, the ferroelectric dipole within the LiNbO₃ becomes polarized, leading to changes in the material's electric state. The polarization switching during the voltage sweep is assessed by measuring the amount of charge that is discharged from the opposite side of the capacitor. This measurement indicates how effectively the ferroelectric material responds to the applied voltage, highlighting the influence of the LiNbO₃ layer thickness on the overall polarization dynamics.

In Figure 6, the relationship between gate voltage and surface potential in a double gate LiNbO₃ NCFET is depicted. As the gate voltage increases, the surface potential also rises, which leads to a more pronounced inversion layer formation. A higher surface potential enables the

inversion layer to form more efficiently and at lower gate voltages, enhancing the transistor's operational performance. This improved operation results in better switching characteristics and reduced power consumption, making the double gate LiNbO₃ NCFET more effective for applications in low-power electronics.

Figure 7 shows the drain current (A) versus gate voltage (V) characteristics for a double gate NCFET structure with varying thicknesses of LiNbO₃ ferroelectric layers (5 nm, 10 nm, 15 nm, and 20 nm). At a constant drain voltage of 1V, the drain current increases as the gate voltage becomes positive, with thinner ferroelectric layers (5 nm) exhibiting higher drain currents and steeper slopes, indicating better performance. This trend suggests that reducing the thickness of the ferroelectric layer improves the device's operational efficiency.

Another crucial factor to take into account is doping the substrate with silicon. NCFET design since the doping concentration causes SS to decrease. To comprehend how an NCFET operates, one must grasp the notion of “capacitance matching,” which forms the foundation of the entire device’s functioning. As illustrated in Figure 8, the subthreshold swing reduces for an increase in ferroelectric layer thickness.

Hysteresis happens as ferroelectric capacitances increase, pushing the device into an unstable zone. The gadget behaves erratically when the ferroelectric components are dense because its capacitance is greater than that of the ferroelectric element. Reducing the ferroelectric thickness could neutralize this. Ferroelectric devices have a steeper slope because of a higher applied voltage and drain current. The subthreshold swing (SS) decreases as the ferroelectric thickness layer in NCFET devices increases, indicating improved device performance. However, increasing the ferroelectric thickness beyond a certain point can lead to hysteresis, which can degrade the transistor’s reliability. Using a double-gate structure helps mitigate this hysteresis, ensuring stable performance. The 5 nm technology is widely adopted in NCFET devices, where a 5 nm ferroelectric thickness demonstrates optimal results. Specifically, NCFETs with a 5 nm ferroelectric layer exhibit 1.22 times higher ON current and 66 times lower leakage current than conventional MOSFETs. This makes NCFETs with a 5 nm ferroelectric thickness ideal for logic circuit design, offering significant improvements in both performance and energy efficiency. The reduced subthreshold swing, combined with higher ON current and lower leakage, makes NCFETs well-suited for modern low-power, high-performance applications. Figure 9 illustrates how subthreshold swing and hysteresis behaviour vary in response to a constant V_{DS} shift.

Figure 9 shows the subthreshold swing (SS) and hysteresis behaviour of the proposed MFMIS DG NCFET structure as the drain-source voltage V_{DS} is swept up to 5V. The black curve represents the minimal SS, which decreases with increasing V_{DS} , while the red curve illustrates the hysteresis voltage, which also decreases as V_{DS} increases. The ferroelectric thickness is maintained at 5 nm, with a maximum drain current of 15 μ A.

Conclusions

In conclusion, the development and implementation of LiNbO_3 -based NCFET signify a substantial advancement in the pursuit of more energy-efficient silicon circuits. By exploiting the negative

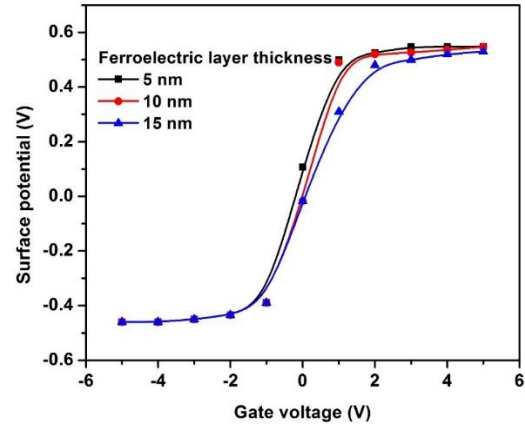


Figure 7. Surface potential with a double gate structure

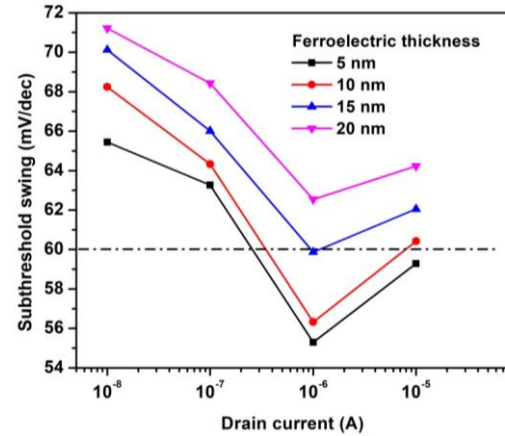


Figure 8. Subthreshold swing with normalized drain current for the proposed MFMIS DG NCFET structure

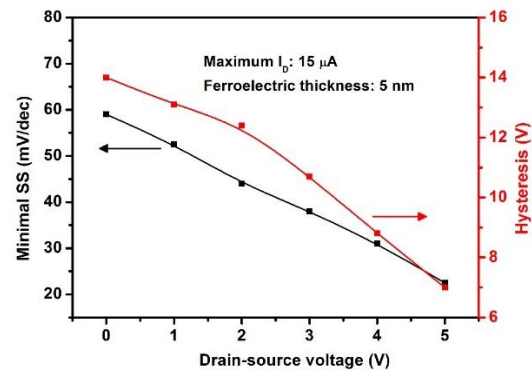


Figure 9 Subthreshold swing and hysteresis curve for the proposed MFMIS DG NCFET structure with V_{DS} swept through 1V

capacitance effect of ferroelectric materials, specifically LiNbO₃, these devices operate at lower voltages, thereby enhancing energy efficiency. The hysteresis-free nature of LiNbO₃-based NCFETs ensures stable and reliable operation, which is essential for the miniaturization and scalability of future semiconductor devices. This study demonstrates that integrating ferroelectric materials with silicon-based transistors can effectively address the energy consumption challenges posed by the Boltzmann limit, paving the way for continued innovation and performance improvements in the semiconductor industry. Future research should focus on further optimizing the ferroelectric properties of LiNbO₃ to enhance the performance of NCFETs. Additionally, exploring other ferroelectric materials and their compatibility with silicon-based devices could provide alternative pathways for improving energy efficiency. Investigating the long-term reliability and operational stability of these devices under varying environmental conditions will be crucial for their practical application. Moreover, scaling down the dimensions of NCFETs and integrating them into complex circuits could unlock new potentials for ultra-low-power electronics, addressing the growing demand for energy-efficient technologies in various applications.

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