

PERFORMANCE ANALYSIS OF WIDE BANDGAP GAN BASED INTERLEAVED CONVERTER FOR CPU VOLTAGE REGULATOR APPLICATIONS

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Abstract

Nowadays, the central processing unit (CPU) of laptop computer operates at very high clock frequencies (GHz) with abrupt load transitions. Therefore, it necessitates an efficient voltage regulator in order to realize the rapid CPU dynamics. In view of this, this paper presents a 4-phase interleaved synchronous buck converter (ISBC) for the CPU applications. It has the exceptional features such as input and output current ripple cancellation, good thermal performance, higher power, current and efficiency. The design of a 9~19 V input, 1 V/45 A, 300 kHz ISBC is accomplished as a CPU voltage regulator. The performance of the converter is interpreted for the line and load regulations based on the voltage mode hysteretic controller. The elaborative PSIM simulation results are presented in view of emphasizing the strength of this controller. Moreover, the efficiency analysis of the Si devices as well as GaN devices based interleaved converter is explored in detail. The GaN devices can ameliorate the power density (PD) as well as efficiency of the ISBC. It also highlights the importance of the switching frequency selection and optimization for the ISBC.

Keywords: Central processing unit; dc-dc converter; modeling; control; GaN devices; efficiency optimization

Introduction

Today it is necessary to design an efficient switched mode power supply for the laptop computer applications. For faster computations, higher clock frequencies (GHz) are required by the central processing unit (CPU) and results in more power consumption (Yan *et al.*, 2024). Hence, the microprocessors CPU core voltage is reduced to around 1 V in view of minimizing the power consumption. These aspects necessitate the stringent requirements in terms of the voltage regulation and converter dynamics. The laptops are powered by the

combination of the battery pack and the AC adapter. The 19 V is obtained from the ac adapter and the battery pack voltage varies from 8.7 V~16.8 V. Therefore, it is required to convert 8.7 V~19 V range voltage to 1 V as required by the CPU. Hence, a suitable DC-DC converter is required for actualizing the efficient power conversion. In CPU Voltage Regulator Module (VRM) applications, the buck topology is not suited for higher switching frequency operation due to the narrow duty cycle problem. Importantly, the PWM controllers impose

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limits on the minimum achievable duty cycle along with the EMI effects on the narrow gate pulses. Another important hurdle is the current-sensing when the VRM is implemented with the average current mode control strategy. In addition, the switches operate in the linear region for most of the time and thereby enriching the switching and on-state losses. The cascading of two buck converters is suitable only for low level currents or else it degrades the efficiency of the converter (Fei *et al.*, 2017). Due to gross mismatch in the turn's ratio, it is difficult to design a high frequency transformer in case of the isolated topologies. The favorable duty cycle range is achieved by the tapped-inductor buck converter (Kaiwei *et al.*, 2005). But it generates voltage spikes and also a moving RHP zero with the load. The active-clamp topology necessitates a well-designed magnetic core structure (Xu *et al.*, 2001a). The forward topology entails the demagnetization of the core with the help of a reset winding (Guo, 2003). In push-pull buck converter the transformer design is critical and may prone to transformer saturation (Xu *et al.*, 2001b). The higher switching loss, conduction loss and reverse recovery loss inducing in case of half-bridge topologies can impede their usage in high current applications (Jia and Lee, 2005; Zhihua *et al.*, 2005). A comparative simulation analysis on various dc-dc converters is presented elaborately for the CPU VRM applications (Yadlapalli and Kotapati, 2014). The quadratic buck converter features in good dynamic performance but with bounded efficiency (Yadlapalli and Kotapati, 2014; Yadlapalli and Kotapati, 2020). A compromise is imperative between the CPU dynamics and efficiency. However, the QBC performance should be heightened further in view of achieving stringent targets with the substantiation of the resonant switching concepts. Another coupled inductor based Half Bridge (HB) converter can bag faster load transitions but with increased number of components (Rakesh *et al.*, 2008). On the other hand, the full bridge converter is designed for getting good dynamics (Rakesh *et al.*, 2010; Rakesh *et al.*, 2012; Kutkut *et al.*, 1995). It has turned out with lower efficiency as compared to the other topologies. On the other hand, the multiphase synchronous buck converter (MSBC) can enable good ripple cancellation effect (Abu-Qahouq *et al.*, 2002; Wang and Tzou, 2007; Jahanbakhshi and Etezadinejad, 2019). Moreover, the transient response is improved with lower inductance and also helps to minimize the output capacitance. But, the downside is the poor ripple cancellation effect at narrow duty cycles. Therefore, the make use of

a MSBC interconnected with smaller inductance is compromised. The increase in current ripple at narrow duty cycles causes more switching and conduction losses. This degrades the efficiency of the MSBC. Hence, a trade-off is required between the efficiency and the transient response. Therefore, this paper presents the simulation analysis of a 4-phase interleaved synchronous buck converter (ISBC) with voltage mode hysteretic controller (VMHC) for the CPU VRM applications. Moreover, the efficiency can be predominantly improved with the incorporation of GaN devices as compared to the Si devices based ISBC (Yadlapalli *et al.*, 2021; Prajapati and Balamurugan, 2023). The GaN devices can operate at higher switching frequencies besides the superior improvement in the power density (PD) of the VRM. It also garners MATLAB programming based exhaustive efficiency analysis for the Si devices as well as GaN devices based ISBC. This work also carries out the switching frequency optimization of the interleaved dc-dc converter.

The main objectives of this paper are as follows

- It describes the important features and characteristics of the ISBC.
- It presents the modeling of the ISBC along with their control aspects.
- It focuses on the ISBC dynamic analysis with respect to the faster load as well as line voltage transitions.
- It also emphasizes the efficiency analysis and switching frequency selection of the Si and GaN devices based ISBC.

The organization of this paper, Section 2 presents the power circuit architecture of the interleaved dc-dc converter, Section 3, Section 4 and Section 5 explores the mathematical modeling, control and loss analysis of the ISBC. Section 6 highlights the exhaustive simulation study along with the efficiency estimation and switching frequency optimization. Finally, Section 7 gives the conclusions.

Power circuit architecture

The schematic of a 4-phase ISBC is depicted in Figure 1. This topology can curtail the current ripples and also enhances the transient response through paralleling of several MSBCs (Abu-Qahouq *et al.*, 2002; Jahanbakhshi and Etezadinejad, 2019; Wang and Tzou, 2007). Importantly, this converter can aggrandize the thermal performance as well as the efficiency. The total current ripple in a 4-phase interleaved VRM is given by equation (1).

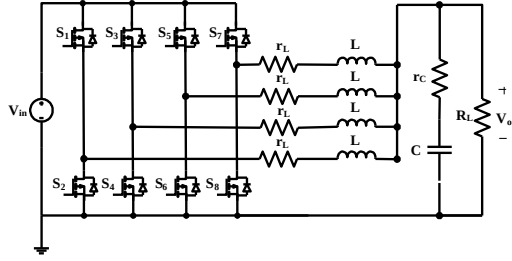


Figure 1. Four phase interleaved synchronous buck converter (ISBC)

$$\Delta I_L = \frac{(V_{in} - V_{out})V_{out}}{8 \cdot V_{in} \cdot f_{sw} \cdot L} \quad (1)$$

Where 'D' is the duty cycle, V_{out} is the CPU voltage, f_{sw} is the operating frequency and ΔI_L is the total inductor current ripple. The total output current ripple decreases with raised phase number and thereby assists in minimizing the output capacitance value.

The output voltage ripple in a 4-phase interleaved VRM is presented by

$$\Delta V_O = \frac{(V_{in} - V_{out})V_{out}}{256 \cdot V_{in} \cdot f_{sw}^2 \cdot L \cdot C} \quad (2)$$

Mathematical modeling of ISBC

The dynamics of an ISBC is evaluated based on the state-space averaging technique (Yadlapalli and Kotapati, 2020; Yang *et al.*, 2024). The issues under interpretation are the input voltage and load current variations. It is made possible through mathematical modeling of the multi-phase ISBC. The ISBC can be viewed as a linear time variant (LTV) system over one switching period. The differential equations are formed during the turn-on and turn-off of the switch.

As mentioned earlier, the literature spotlights the state-space averaging methodology (SSAM) based converter modeling. This SSAM can accentuate the different control transfer functions (TFs) of the ISBC based on equation (3).

$$\begin{aligned} \frac{d\tilde{x}(t)}{dt} &= A_{Ms}\tilde{x}(t) + B_{Ms}\tilde{u}(t) + B_{Mi}\tilde{d}(t) \\ \tilde{y}(t) &= C_{Ms}\tilde{x}(t) + E_{Ms}\tilde{u}(t) + E_{Mi}\tilde{d}(t) \\ A_{Ms} &= A_{M1}D + A_{M2}(1-D) \\ B_{Ms} &= B_{M1}D + B_{M2}(1-D) \\ C_{Ms} &= C_{M1}D + C_{M2}(1-D) \\ E_{Ms} &= E_{M1}D + E_{M2}(1-D) \\ B_{Mi} &= (A_{M1} - A_{M2})X + (B_{M1} - B_{M2})U \\ E_{Mi} &= (C_{M1} - C_{M2})X + (E_{M1} - E_{M2})U \end{aligned} \quad (3)$$

The small ac variations of the state vector, input vector, output vector and duty cycle are represented by $\tilde{x}(t)$, $\tilde{u}(t)$, $\tilde{y}(t)$, $\tilde{d}(t)$.

The appropriate small signal TFs are procured from equation (4) by applying Laplace transformation to equation (3).

$$\begin{aligned} \tilde{x}(s) &= [(SI - A)^{-1}B_{Ms} \quad (SI - A)^{-1}B_{Mi}] \begin{bmatrix} \tilde{u}(s) \\ \tilde{d}(s) \end{bmatrix} \\ \tilde{y}(s) &= [C_{Ms}(SI - A)^{-1}B_{Ms} + E_{Ms} \quad C_{Ms}(SI - A)^{-1}B_{Mi} + E_{Mi}] \begin{bmatrix} \tilde{u}(s) \\ \tilde{d}(s) \end{bmatrix} \end{aligned} \quad (4)$$

It is so essential to throw light on the assumptions made while modeling the ISBC. The converter switching frequency (f_{sw}) should be predominantly greater than the natural frequency (f_r) of the ISBC. This tends to eliminate higher order harmonics associated with the system dynamics. It means that the first order linear ac terms are considered and further neglecting the higher order nonlinear ac terms. Here, the ac variations are assumed to be much smaller than the quiescent values as represented below.

$$\begin{aligned} \tilde{x}(s) &\ll X \\ \tilde{y}(s) &\ll Y \\ \tilde{u}(s) &\ll U \\ \tilde{d}(s) &\ll D \end{aligned}$$

Where, X, Y, U, D are the equilibrium (dc) state vector, output vector, input vector and duty cycle. As shown in Figure 2, the non-idealities such as dc resistances (DCRs) and equivalent series resistance (ESR) of all the inductors and output capacitor are considered during the modeling of the ISBC. These are designated as r_L and r_C .

The vital control signal-to-output voltage TF for the dynamic analysis of the ISBC based on equation (4) is given by $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$.

As explained before, it is significant to derive the control TFs for the stability assessment of the ISBC. It includes the evaluation of the phase margin (PM) and gain margin (GM) of the ISBC. The simulation associated case studies are fulfilled with the implementation of the voltage-mode hysteretic control (VMHC) based ISBC. In most of the practical cases, the GM and PM of the VMHC based ISBC are expected to be 6 dB and 45° against the input dc voltage fluctuations, power component tolerances, temperature changes and saturation effects. The transient settling time and voltage deviation are the performance indices interconnected with the dynamic analysis of the ISBC. The output voltage should come to steady state after encountering the step-up or step-down load transient disturbances. The output voltage may rise or fall with respect to the above conditions. Smoother operation is possible through proper selection and tuning of the proportional Integral (PI) controller parameters.

The TF of the control signal-to-output voltage is given by equation (5) based on the equation (4).

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_{in}R_Lr_c}{L(R_L+r_c)} \left[\frac{s + \frac{1}{Cr_c}}{s^2 + s\left(\frac{C(R_Lr_c + R_Lr_L + r_cr_L) + L}{LC(R_L+r_c)}\right) + \frac{R_L+r_L}{LC(R_L+r_c)}} \right] \quad (5)$$

Voltage mode control strategy

The basic voltage-mode control (VMC) based ISBC is illustrated in Figure 2. This control approach can be enlightened with the aid of only one control loop. The ISBC output voltage and reference value are compared and the error is processed to the PI controller. Moreover, the pulse width modulation (PWM) pulses are generated in order to turn-on and turn-off of the switching devices. However, this research work relies on the VMHC in view of rendering the good converter dynamics.

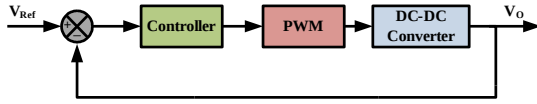


Figure 2. Illustration of VMC based ISBC

Efficiency analysis

The MOSFET switches are employed due to the high switching frequency operation of the converter (Ravindranath *et al.*, 2023). The on-state loss of the each MOSFET is given by

$$P_{MOSFETs,Conduction} = (I_{rms}^2 * R_{ds}) \quad (6)$$

Where I_{rms} is the rms current and R_{ds} is the on-state resistance of each MOSFET.

The conduction losses of each inductor can be found as

$$P_{L,ConductionLoss} = (I_{Lrms}^2 * R_{DCR}) \quad (7)$$

The conduction losses of output capacitor is estimated as

$$P_{C,ConductionLoss} = \frac{\Delta I_L^2 R_{ESR}}{12} \quad (8)$$

Where, ΔI_L , DCR and ESR are the inductor current ripple, inductor DC resistance and equivalent series resistance of the capacitor.

The output capacitor losses can be calculated as

$$P_{Outputcapacitor} = \frac{V_{sw}^2 f_{sw} C_{oss}}{2} \quad (9)$$

Where V_{sw} is peak switch voltage and C_{oss} is the MOSFET output capacitance.

The gate power losses are computed as

$$P_{Gate} = (V_{DD} f_{sw} Q_G) \quad (10)$$

Where, Q_G and V_{DD} are the gate charge and voltage at the drain side.

The MOSFETs switching losses are given by

$$P_{sw} = \frac{V_{sw} I_{pk}}{2} f_{sw} (t_{on} + t_{off}) \quad (11)$$

Where I_{pk} is peak value of the switch current, t_{on} and t_{off} are the on-time and off-time of the switch. The reverse recovery losses are given by

$$P_{rr} = (V_{sw} Q_{rr} f_{sw}) \quad (12)$$

Where, Q_{rr} is the reverse recovery charge of the MOSFET.

The total losses of the ISBC are given by

$$P_T = (P_{Conduction} + P_{Switching} + P_{Reverse recovery} + P_{OutputCapacitor} + P_{Gate}) \quad (13)$$

As switching frequency increases, the size and cost of the passive components decreases with a concomitant improvement in the power converter dynamics. But the converter efficiency gets diminished with respect to the switching frequency. In practice, the agreeable switching frequency range is selected in view of grabbing the trade-off between the achievable PD and the converter efficiency. Hence, this research work also emphasizes the effect of switching frequency on the converter efficiency. The exhaustive efficiency analysis of the ISBC is presented with the aid of Si and GaN devices.

Simulation Results

Table 1 presents the simulation parameters of the 4-phase ISBC as a VRM for the CPU. A 9 V ~19 V, 1 V/45 A, 300 kHz 4-phase ISBC is designed and simulated based on the VMHC as shown in Figure 3. The GaN switches are selected from EPC Company with an on-state resistance of 1.45 mΩ. The capacitor has an ESR of 8 mΩ. The bode diagram of the control signal-to-output voltage is shown in Figure 4.

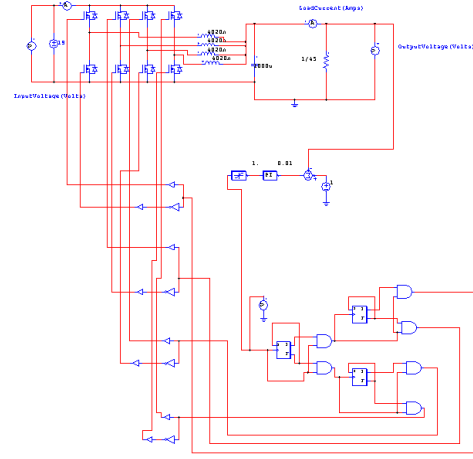
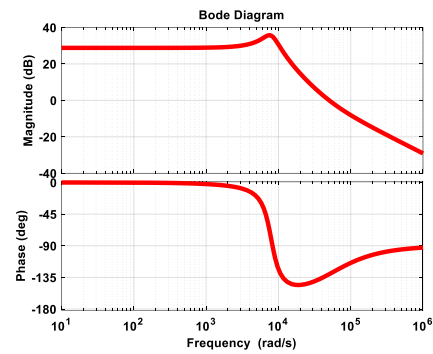
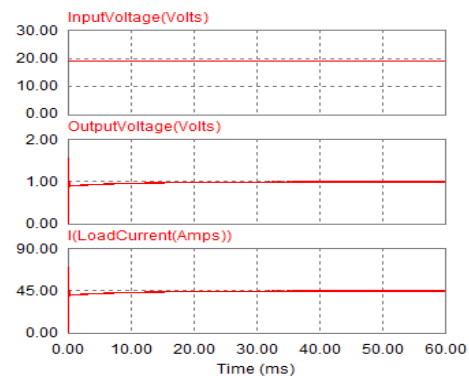
Table 1. Converter specifications

Nominal Parameter	Value
V_{in}	9 V ~19 V
L_1, L_2, L_3, L_4	4.02 μ H
C	1000 μ F
f_{sw}	300 kHz
V_o	1 V
P_o	45 W
K_p and K_i	1 & 0.1

The continuous conduction mode (CCM) operation based ISBC has several attractive features such as low current ripple, reduced conduction losses, switching losses and high efficiency as compared to the discontinuous conduction mode (DCM) operation. On the other hand, the design of a CPU VRM imposes stringent limits on the allowable current and voltage ripples of the passive elements. This work aims the inductor current ripple (ΔI_L) and capacitor voltage ripple (ΔV_O or ΔV_C) are to be around 15-20% and $\leq 3\%$. The L and C values are chosen at least 20-25% higher than the critical inductance and capacitance values. Moreover, the performance of the ISBC is optimized with a switching frequency (f_{sw}) of 300 kHz and greater than resonant frequency (f_r) with 2.517 kHz. The higher switching frequencies can enhance the ISBC transient performance as well as the PD but with a concomitant effect of deteriorating the efficiency. On the other hand, the design of the Propotional Integral (PI) controller is effectuated with the help of MATLAB/SISO tool based on the control TF given by equation (6). This approach includes the various steps associated with the selection of the architecture, system data and finally graphical tuning. The pole and zero locations are adjusted until the system ensures small signal stability and good steady state response. Moreover, with proper tuning the large signal stability can be grabbed against the parameter variations, load turbulences and component tolerances. The propotional gain (K_p) and integral gain (K_i) of the PI controller are obtained as 1 and 0.1. The stability margins are nearby 6 dB and 45° .

Figure 5 presents the VHMC based 4-phase ISBC output voltage (V_{Out}) and load current (I_O) waveforms at an input voltage (V_{in}) of 19 V. The corresponding output voltage settles very quickly and reaches steady state with a negligible steady state voltage ripple (SSVR). Figure 6 shows the magnified waveform of Figure 5. The SSVR is predominantly less than 1%. As per the IEEE standards the SSVR should be in the proximity range of 3% - 5%. This emphasizes the good steady

state performance of the VHMC based 4-phase ISBC as a CPU VRM.

**Figure 3. PSIM Simulation circuit of VHMC based 4-phase ISBC****Figure 4. Bode diagram of control signal-to-output voltage****Figure 5. VHMC based 4-phase ISBC steady state output voltage and current waveforms at 19V V_{in}**

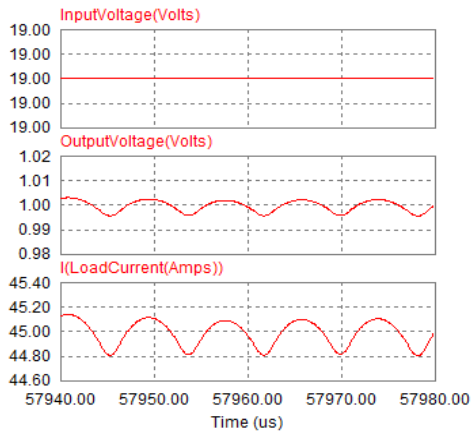


Figure 6. VPMC based 4-phase ISBC magnified steady state V_{Out} and I_{Out} waveforms at 19V V_{in}

Figure 7 presents the VPMC based 4-phase ISBC V_{Out} and I_{Out} waveforms at an V_{in} of 9 V. The output settles very quickly and reaches steady state with a negligible SSVR of less than 1% and meeting the IEEE standards. Figure 8 shows the magnified waveform of Figure 7. This simulation study is to highlight the practical scenario when the input ac voltage encounters a steady voltage dip or the Lithium-ion battery pack is at the lower discharge voltage of 9 V under spontaneous utility grid power failure occurrences. Even then the converter will be able to maintain the constant output voltage of 1 V by regulating the duty cycle of the VPMC based 4-phase ISBC.

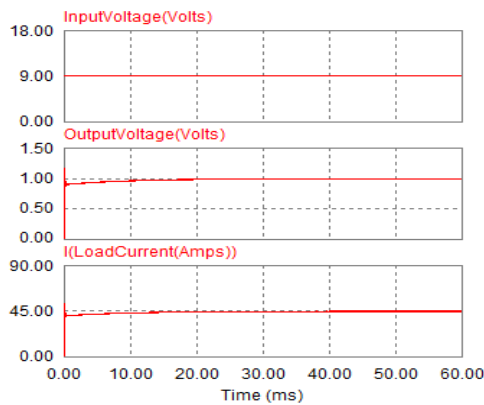


Figure 7. VPMC based 4-phase ISBC steady state output voltage and current waveforms at 9V V_{in}

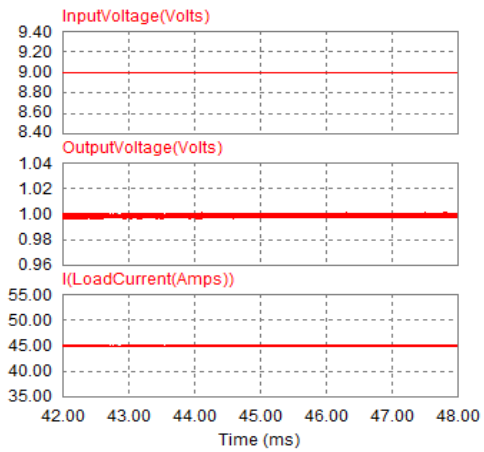


Figure 8. VPMC based 4-phase ISBC magnified steady state V_{Out} and I_{Out} waveforms at 9V V_{in}

Figure 9 shows the step increment in load from 5 A - 45 A at $t=0.05$ sec, having exhibited 20% transient output voltage dip and takes 10 msec to reach 1 V. Figure 10 shows the magnified waveform of Figure 9. As mentioned earlier, the CPU is a high dynamic load and needs good converter dynamics.

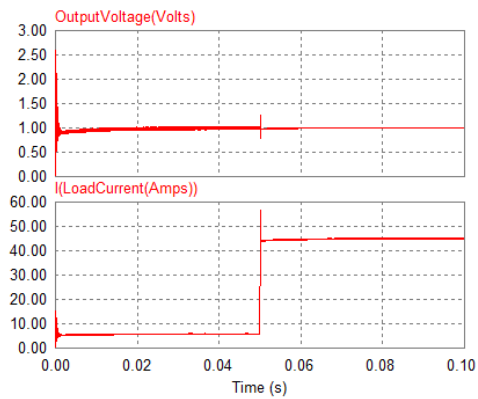


Figure 9. VPMC based 4-phase ISBC V_{Out} and I_{Out} waveforms during load regulation at 19V V_{in}

This simulation study highlights the worst dynamic load transition of the CPU i.e. from the minimum load of 5 A to a maximum load of 45 A. Here, the voltage dip as well as the settling time encountered is little bit far away from the set IEEE

standard value of $\leq 10\%$. The dynamic performance is found to be good and acceptable for this worst step increment in load and the VPMC based 4-phase ISBC has proven the excellent load regulation.

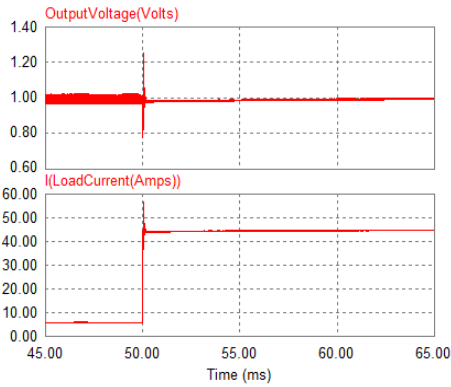


Figure 10. VPMC based 4-phase ISBC magnified V_{out} and I_{out} waveforms during load regulation at 19V V_{in}

Figure 11 shows 19 - 9 V step decrement in V_{in} at $t=0.1$ sec, having exhibited nearly 1% transient output voltage dip as per the IEEE standards and takes 1.0 msec to reach 1 V. This simulation study ensures the worst practical scenario when the input ac voltage encounters the severe under voltage perturbations. As mentioned earlier, the CPU is a high dynamic load and also needs good line regulation. The dynamic performance is found to be good for this step decrement in V_{in} . This has proven the excellent line regulation feature of the VPMC based 4-phase ISBC.

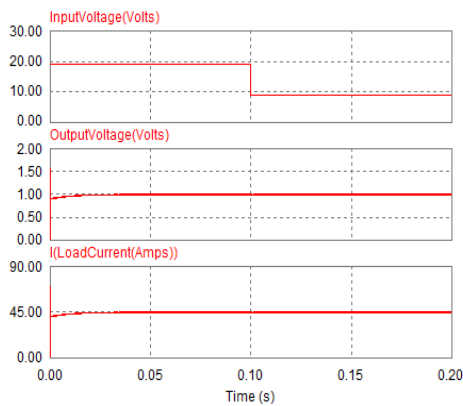


Figure 11. VPMC based 4-phase ISBC V_{out} and I_{out} waveforms during line regulation for 19 V to 9 V step V_{in}

Figure 12 depicts the efficiency Vs load current characteristics for the Si devices based 4-phase ISBC operating at 300 kHz and at input voltages of 19 V, 17 V, 15 V, 12 V and 9 V. A very high ISBC efficiency of 82.1% is realized at an V_{in} of 9 V. The efficiency of the Si devices based 4-phase ISBC is found to be 81.3% at the rated load power of 45 W.

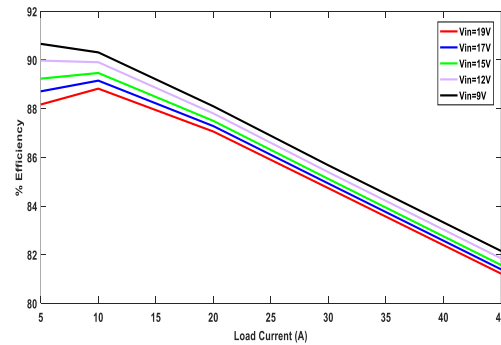


Figure 12. Efficiency Vs load current curves of 4-phase ISBC with Si devices

Figure 13 shows the effect of switching frequency on the efficiency of the Si devices based 4-phase ISBC. The curves are shown for the 100 kHz - 900 kHz switching frequency variation at different load currents of 10 A, 15 A, 20 A, 30 A and 45 A. At rated load current of 45 A, the efficiency of the ISBC changes from 82.7% to 75.0% under the considered switching frequency variation. There is an efficiency change of 7.7% with the Si devices based 4-phase ISBC. A highest efficiency of 76.8% is noticed at the load current of 15 A and 900 kHz.

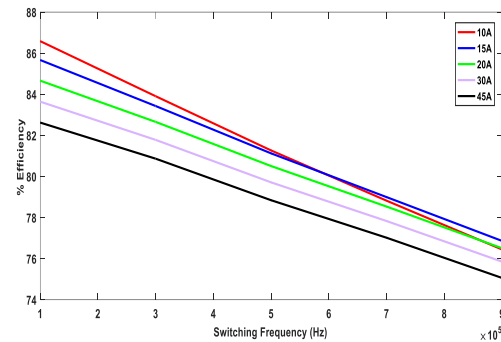


Figure 13. Efficiency Vs Switching Frequency curves of ISBC with Si devices

The various losses distribution is represented in Figure 14 for the Si devices based 4-phase ISBC. The dominant losses are the conduction and switching losses. The switching losses are going to occupy major portion of the total losses. The conduction losses almost remain constant for the switching frequency diversification from 100 kHz to 900 kHz. This may be due to the decreased DCRs of inductors compensated by a rise in the ESR of the output capacitor. On the other hand, the switching loss aggrandizes much more by 56.6% under the considered switching frequency variation as compared to the conduction losses. Thus, higher switching frequencies can curtail the efficiency but with an anonymous betterment of the PD of the ISBC. The other losses such as gate losses, output capacitor losses and reverse recovery losses are relatively negligible with very less than 1 W as compared to the conduction and switching losses.

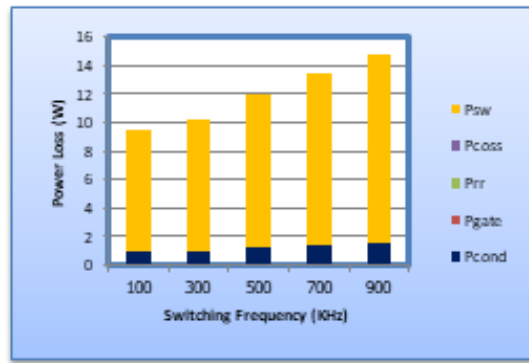


Figure 14. Power loss analysis of 4-phase ISBC with Si devices

Figure 15 depicts the efficiency Vs load current characteristics for the GaN devices based ISBC operating at 300 kHz and at input voltages of 19 V, 17 V, 15 V, 12 V and 9 V. A very high efficiency of 95.5% is noticed at an V_{in} of 9 V. The efficiency of the GaN devices based 4-phase ISBC is found to be 94.5% at the rated load power of 45 W. This efficiency is going to be 14.2% greater than the Si switches based 4-phase ISBC. Thus the efficiency is predominantly improved with the GaN devices based 4-phase ISBC as compared to the Si devices based 4-phase ISBC.

Figure 16 shows the effect of switching frequency on the efficiency of the GaN devices based 4-phase ISBC. The curves are shown for the 100 kHz - 900 kHz switching frequency variation at different load currents of 10 A, 15 A, 20 A, 30 A and 45 A. At rated load of 45 A, the efficiency of

the ISBC changes from 95.3% to 89.1% with respect to the considered switching frequency variation. Thus the GaN switches are superior in improving the efficiency of the power converters especially for the low voltage and high power applications. This analysis gives a clear-cut idea while selecting the switching frequency of the 4-phase ISBC. Hence, a trade-off can be achieved between the transient response and efficiency of the ISBC.

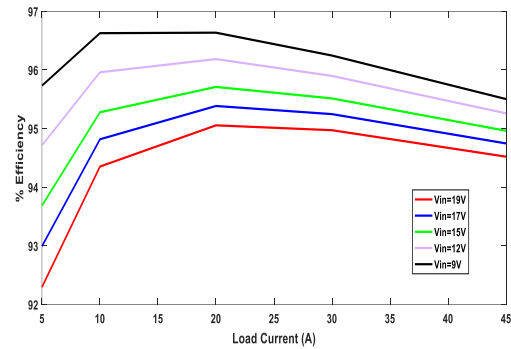


Figure 15. Efficiency Vs load current curves of 4-phase ISBC with GaN devices

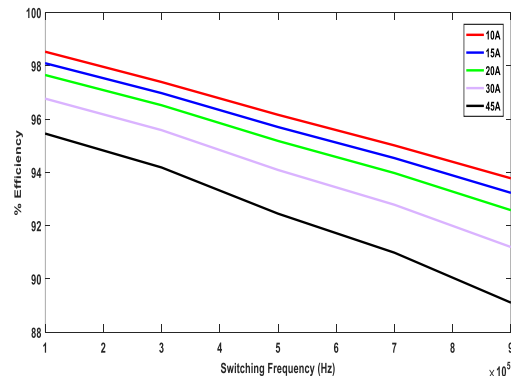


Figure 16. Efficiency Vs Switching Frequency curves of ISBC with GaN devices

The various losses distribution of GaN devices based ISBC is represented in Figure 17 for the switching frequency alteration from 100 kHz to 900 kHz. Here also, the dominant losses are the conduction and switching losses. The switching losses are going to occupy major portion of the total losses. As observed in Figure 17 and Figure 14, the conduction losses with the GaN devices based ISBC decreases by 87.5% and 80% at the respective switching frequencies of 100 kHz and 900 kHz as compared to the Si devices based ISBC. Similarly, the switching losses decreases by 74.7% and 61.5%

with the GaN devices based ISBC as compared to the Si devices based ISBC. As shown in Figure 17 specifically with GaN devices, the switching losses increases by 138.1% as compared to the conduction loss increment of 200% for the switching frequency change from 100 kHz to 900 kHz. Moreover, the other losses such as gate losses, output capacitor losses and reverse recovery losses are found more negligible as compared to the Si devices based ISBC. At the rated load conditions and operating frequency of 45 A and 300 kHz, the efficiency of the GaN devices based ISBC is going to be 14.2% greater than the Si devices based ISBC. Thus, the wide bandgap semiconductor devices not only enhance the efficiency but also can operate at very high switching frequencies due to their extraneous figure of merit products such as $(R_{DS(on)} * E_{oss})$, $(R_{DS(on)} * Q_{rr})$ and $(R_{DS(on)} * Q_c)$ as compared to the Si devices. This tends to aggrandize the PD of the ISBC. However, the GaN device technology is suffering from the issues such as cross talk, thermal management, package materials, reliability and PCB design. Table 2 enlightens the obtainable efficiency comparison for both the Si and GaN devices based ISBC.

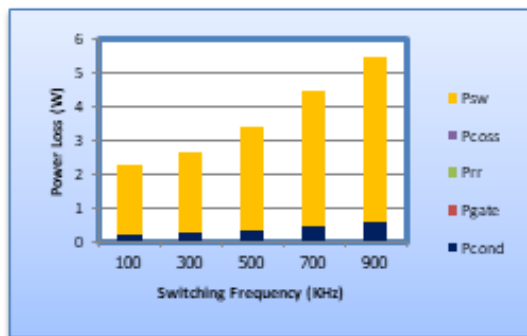


Figure 17. Power loss analysis of 4-phase ISBC with GaN devices

Table 2. Efficiency comparison of ISBC with Si and GaN devices

	Si devices based ISBC	GaN devices based ISBC
% Efficiency at rated load conditions	81.3	94.5
% Efficiency Maximum achievable	82.1	95.5
% Efficiency change for 100 kHz - 900 kHz switching frequency variation at rated load conditions	7.7	6.2

Conclusions

This paper emphasizes the significant features of the 4-phase ISBC for the CPU VRM applications. This ISBC is designed and simulated with the incorporation of voltage mode hysteretic controller (VMHC). The results highlight that the converter dynamics are good with the VMHC based 4-phase ISBC during the step-increment in load as well as the step-decrement in input voltage. The 4-phase ISBC has exhibited the good dynamics during the load and line regulations with a settling time of few msec and are in line with the IEEE standards. In addition, this 4-phase ISBC has shown the good efficiency at the rated load current of 45 A. The incorporation of GaN devices based ISBC has resulted in an efficiency enhancement of 14.5% at the rated load conditions as compared to the Si devices based ISBC. For the switching frequency variation from 100 kHz - 900 kHz, the observed efficiency change is from 95.3% to 89.1% for the GaN devices based ISBC as compared to the Si devices based ISBC with variation from 82.7% to 75.0%. There is an abundant scope to extend this simulaion work for further higher power levels of the ISBC.

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Acronym	Abbreviation
SSVR	Steady state voltage ripple
CPU	Central processing unit
ISBC	Interleaved synchronous buck converter
PD	Power density
VRM	Voltage regulator module
PWM	Pulse width modulation
EMI	Electromagnetic interference
RHP	Right half plane
MSBC	Multiphase synchronous buck converter
VHMC	Voltage mode hysteretic controller
LTV	Linear time variant
SSAM	State-space averaging methodology
TF	Transfer function
PI	Proportional integral
DCR	Dc resistance
ESR	Equivalent series resistance
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
SISO	Single input and single output
Symbol	Description
V_{out} or V_o	Output voltage, V
I_o or I_{out}	Load current, A
V_{in}	Input voltage, V
f_{sw}	Switching frequency, Hz
R_L	Load resistance, Ω
C	Capacitance, F
L	Inductance, H
D	Duty cycle
ΔI_L	Inductor current ripple, A
ΔV_o or ΔV_c	Capacitor voltage ripple, V
K_p	Proportional gain
K_i	Integral gain
V_{sw}	Peak switch voltage, V
Q_{rr}	Reverse recovery charge, C
P_r	Reverse recovery loss, W
I_{pk}	Peak switch current, A
t_{on}	On time, Sec
t_{off}	Off time, Sec
P_G or P_{Gate}	Gate power losses, W
Q_G	Gate charge, C
V_{DD}	Drain voltage, V
C_{OSS} or C_o	Output capacitance, F
P_{ocss}	Output capacitor losses, W
P_c	Capacitor conduction losses, W
P_L	Inductor conduction losses, W
I_{rms}	Rms current, A
$P_{C-MOSFET}$	MOSFET conduction losses, W
P_{sw}	Switching losses, W
P_o	Output power, W
$\mathbf{u}(t)$	Small ac variations in input vector
$\mathbf{d}(t)$	Small ac variations in duty ratio
$\mathbf{x}(t)$	Small ac variations in state vector
$\mathbf{y}(t)$	Small ac variations in output vector
X	Equilibrium (dc) state vector
Y	Equilibrium (dc) output vector
U	Equilibrium (dc) input vector
D	Equilibrium (dc) duty cycle
A, B, C, D, E	Matrices
r_L	Dc resistance of inductor, Ω
r_c	Equivalent series resistance of capacitor, Ω
R_{DS}	Drain to source on resistance, Ω
E_{OOS}	Output capacitance stored energy, J
M	Matrix
S	State-space
i	Input duty
f_r	Resonant frequency, kHz