

A MODIFIED CONTROL SCHEME TO MITIGATE HARMONICS, IMPROVE VOLTAGE REGULATION & POWER FACTOR USING SINGLE-PHASE SHUNT ACTIVE POWER FILTER

Jotirmoy Samanta¹, Ralli Sangno² and Rajen Pudur^{3,*}

Received: March 02, 2024; Revised: November 05, 2024; Accepted: December 02, 2024

Abstract

This paper presents a modified control scheme to eliminate various power quality issues using a single-phase shunt active power filter (SAPF). The focus is primarily on harmonics mitigation, power factor (PF) correction, DC link voltage regulation, and reducing the settling time of the system. A nonlinear PID (NLPID) controller is employed to regulate the DC link voltage and reduce the system's settling time. The overall system is modeled for a 1 kW load and tested under 85% load condition. The results, obtained using the MATLAB/Simulink platform, are found to be quite satisfactory. After compensation, the total harmonic distortion (THD) is reduced to below 8%, in compliance with the IEEE 519-2022 standard, and the PF is improved to nearly unity.

Keywords: Harmonics reduction; Power factor improvement; Power quality; Shunt Active Power Filter

Nomenclature

V_S	Peak Source voltage
$V_{(RMS)}$	Source voltage RMS
V_C	DC- link capacitor voltage
v_a, v_b, v_c	Three phase source voltage
U_a, U_b, U_c	Unit vectors in phase with v_a, v_b, v_c
w_a, w_b, w_c	Unit vectors in quadrature with v_a, v_b, v_c
SAPF	Shunt Active Power Filter
PF	Power Factor
THD	Total Harmonics Distortion
NLPID	Non- linear PID

Introduction

Power system is facing drawbacks majorly in transferring bad power. Bad power is nothing but fluctuation in voltage, harmonics in the waveforms, low PF, etc. Power quality issues like harmonics distortion and poor PF occurs mainly when the loads are non- linear and inductive in nature. The power quality issues definition and the relation between different issues are elaborated in (Cividino, 1992; Grady and Gilleskie, 1993). To increase the efficiency of the system and supply good power, supply should be pure sinusoidal, 230 V RMS

Department of Electrical Engineering, NIT Arunachal Pradesh, Jote, India. E-mail: samanta.jotirmoy@gmail.com; ralli@nitap.ac.in; rajenpudur@nitap.ac.in*

* Corresponding author

DOI: <https://doi.org/10.55766/sujst-2024-06-e03764>

Suranaree J. Sci. Technol. 31(6):010343(1-7)

(for single phase), 50 Hz with power factor of 0.95 to 1. SAPF is a device which can introduce compensation current to the system and rectify the power quality issues.

The design of the single phase SAPF is stated in (Singh *et al.*, 2004; Biricik *et al.*, 2016); (Jayasankar and Vinatha, 2020). There are different techniques to control SAPF and it is categorised into three domain they are time, frequency, and soft computing domain (Kumar and Bansal, 2018). The conventional method of generating the reference current of SAPF are in time domain by using instantaneous active and reactive power theory and synchronous reference frame theory techniques. The details of both the techniques are elaborated in (Khadkikar *et al.*, 2010; Monfared *et al.*, 2013; Angélico *et al.*, 2014; Gautam *et al.*, 2014; Magdum and Patil, 2017; Imam *et al.*, 2020). Among the control schemes under time domain the synchronous reference frame theory found to be the best for THD reduction. (Samanta and Pudur, 2022). Hence this technique is used to solve multiple power quality issues by considering induction generator as source (Samanta *et al.*, 2024a). Apart from these techniques there are also other techniques to control SAPF by using digital deadbeat controller, self-tuning method, neural network, adaptive backstepping etc. which is discussed in (Komurcugil and Kukrer, 2006; Karbasforooshan and Monfared, 2020; Son *et al.*, 2017; Salimi *et al.*, 2017; Fei *et al.*, 2021; Ouchen *et al.*, 2020). Also, some of the techniques are hybridised and modified to solve multiple power quality issues (Jayasankar and Vinatha, 2020; Karbasforooshan and Monfared, 2020; Ouchen *et al.*, 2020). An improved and new control algorithm was proposed by A. Chandra *et al.* in the year 2000 to control SAPF, through which multiple power quality issues like harmonics elimination, PF

correction, voltage regulation can be successfully solved (Chandra *et al.*, 2000). Later the control algorithm was used to solve power quality issues in induction generator (Singh *et al.*, 2006); (Chauhan *et al.*, 2010). Including the power quality issues discussed by (Chandra *et al.*, 2000) the settling time of DC link capacitor can also be reduced by using NLPID proposed in (Zaidner *et al.*, 2010). In NLPID it is found that using only proportional controller the peak voltage of DC can also be reduced (Wang *et al.*, 2015). Based on NLPID SRF theory is modified for single phase system and reported settling time of 0.08 sec. (Samanta *et al.*, 2024b).

After brief literature survey it is found that SAPF can solve multiple power quality issues by controlling and generating its reference current. Due to various power quality issues the efficiency of the system decreases, the cost of electricity increases and also the life span of the equipment is reduced. So, this disadvantage will also affect the residential areas where single phase is available. The primary goal of this paper is to address various power quality issues concurrently within a single-phase household system. The modified control scheme is specifically designed to tackle key challenges, including harmonic reduction, power factor correction, minimizing settling time, and regulating the DC voltage of the SAPF. The work presented in this paper reported the lesser settling time of the DC link voltage than the previous works. The circuit diagram of the whole system is shown in Figure 1.

This paper is organized into five sections. Section I provides an introductory overview. Section II outlines the design parameters, while Section III details the control system. Section IV presents and discusses the simulation results, and finally, Section V offers the conclusion of the study.

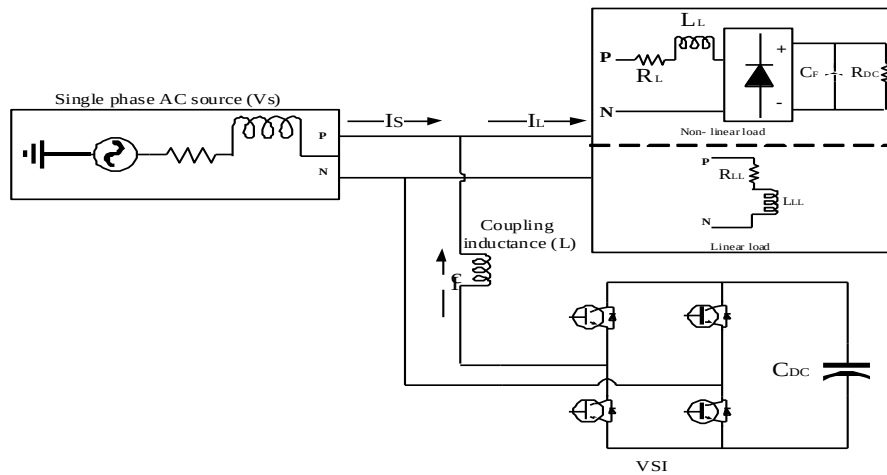


Figure 1. System circuit diagram

Design of SAPF:

SAPF is composed of one inverter where by giving gate pulse to the inverter switches the compensating current can be controlled. To filter the output of the inverter, filters are used. Generally coupling inductor is preferred for filtering the output of inverter. In the DC side of inverter DC source may be used but if the inverter is working only as SAPF then DC- link capacitor is preferred. The DC- link capacitor voltage must be greater than the peak voltage of the source and can be estimated by using equation (3), where m is modulation index which can be considered as 1 (Singh *et al.*, 2004). Also, the maximum and minimum limit of DC- link voltage can be determined from equations (1) and (2) (Biricik *et al.*, 2016).

$$V_{C(max)} = 1.5\sqrt{2} V_s \quad (1)$$

$$V_{C(min)} = \sqrt{2} V_s \quad (2)$$

$$V_C = \frac{2\sqrt{2}(\frac{V_s}{\sqrt{3}})}{m} \quad (3)$$

The DC- link capacitor plays a vital role in SAPF. It should design in such a way that the SAPF should be capable of delivering instantaneous energy during sudden loading condition. The energy required during transients and to provide reactive power to the source can be calculated by using equation (4), and maximum range of energy can be obtained by equation (5). The main role of the capacitor in SAPF is to provide real power to the load. So, the capacitor value can be obtained by using equation (6), where $\bar{P}$ is the harmonic power to be provide by SAPF, ΔV_{DC} is ripple voltage acceptable value and ω is angular frequency (Biricik *et al.*, 2016). But considering 8% dip in DC voltage the capacitor value is determined from equation (7). To reduce ripple voltage and to avoid resonance effect, DC- link capacitance must be between 0.5 to 0.7 p.u. or greater than 0.9 p.u. (Singh *et al.*, 2004).

$$E = V_{(RMS)} I_{(RMS)} t \quad (4)$$

$$E_{max} = P_{max} t \quad (5)$$

$$C_{DC} = \frac{\bar{P}}{\omega V_C \Delta V_{DC}} \quad (6)$$

$$C_{DC} = \frac{2E_{max}}{V_C^2 - V_{C(min)}^2} \quad (7)$$

The inductance required in SAPF is evaluated from equation (8), where $h, f_{s(max)}$ denotes hysteresis band and maximum switching frequency.

Hysteresis band is generally considered 5% of the compensating current I_c . Also, it should be within a range (0.05 to 0.15) of compensating current (Biricik *et al.*, 2016; Jayasankar and Vinatha, 2020).

$$L = \frac{V_C}{4hf_{s(max)}} \quad (8)$$

Control Scheme of SAPF

The modified control scheme obtains in-phase components and quadrature component of the supply reference current. In this technique two NLPID controllers are used to regulate DC- link voltage and PF. The three-phase control scheme proposed by (Chandra *et al.*, 2000) is converted to single phase system. For single phase system the source voltage is first sensed and then the RMS value of it is calculated. Then the source voltage is converted to three phase system by giving phase difference of 120° as shown in equations (9-11). The block diagram of these equations is given in Figure 2(a).

$$v_a = \sqrt{2} V_{(RMS)} \sin(\omega t) \quad (9)$$

$$v_b = \sqrt{2} V_{(RMS)} \sin(\omega t + 120^\circ) \quad (10)$$

$$v_c = \sqrt{2} V_{(RMS)} \sin(\omega t - 120^\circ) \quad (11)$$

Now the amplitude of the sensed sinusoidal source voltage is computed by using Eq. 12. Then the unit vectors which is in phase with v_a are computed by (13). Now, with help of quadrature transformation the unit vectors which is in quadrature with v_a, v_b, v_c can be determined as shown in equation (13).

$$V_p = \sqrt{\frac{2}{3} (v_a^2 + v_b^2 + v_c^2)} \quad (12)$$

$$U_a = \frac{v_a}{V_p} \quad (13)$$

$$w_a = -\frac{v_b}{\sqrt{3}} + \frac{v_c}{\sqrt{3}} \quad (14)$$

The error of DC- bus voltage is computed using equation (15), where $V_{DC(ref)}$ is the reference DC voltage. Then it is tuned by using NLPID controller. The generalised equation of NLPID is represented in equation (16) (Zaidner *et al.*, 2010).

$$\Delta V_{DC} = V_{DC(ref)} - V_{DC} \quad (15)$$

$$\bar{u} = K_p \Psi(x, \alpha, \delta) \quad (16)$$

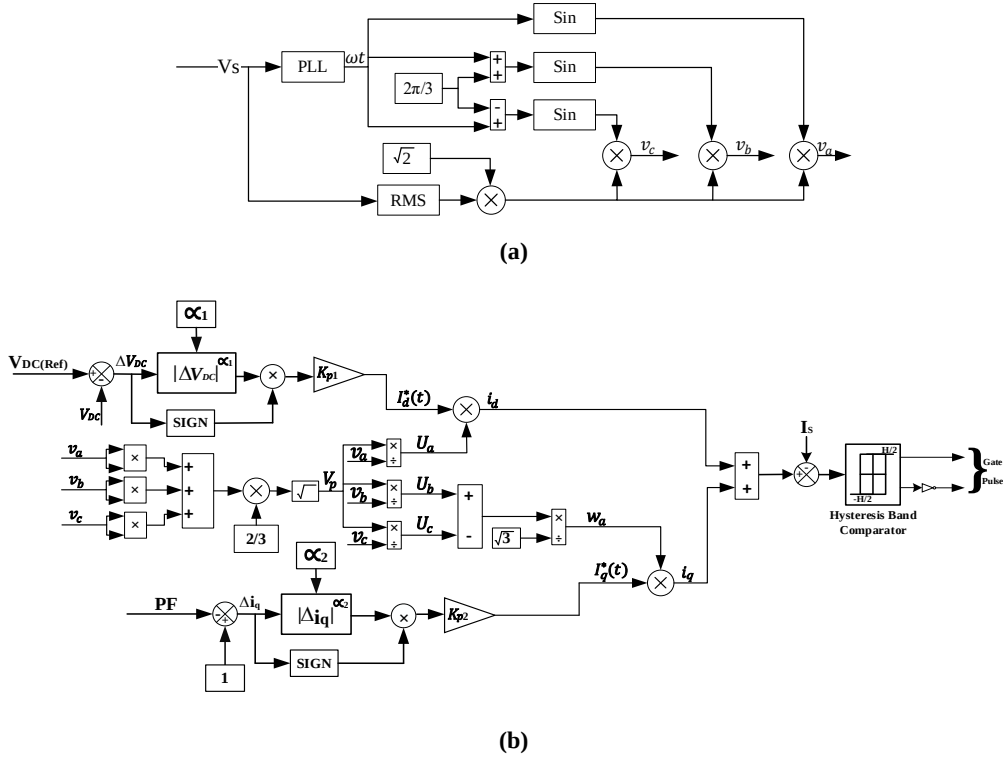


Figure 2. (a) Single phase to three phase conversion, (b) Modified control scheme block diagram

where,

$\bar{u}$ is $I_d^*(t)$ and $I_q^*(t)$

$\Psi(x, \alpha, \delta)$ can be defined as:

$$\Psi(x, \alpha, \delta) = \begin{cases} |x|^\alpha \cdot \text{Sign}(x), & \text{when } |x| > \delta \\ \delta^{\alpha-1} \cdot x, & \text{when } |x| \leq \delta \end{cases}$$

where x is defined as the error of the DC voltage (i.e. ΔV_{DC}) and the error of quadrature current (i.e. Δi_q).

Finally the direct and quadrature current can be modified as equations (17, 18). The reference current (I_c) is generated by summing up the in-phase component and quadrature component of the source reference current as shown in equation (19).

$$i_d = U_a I_d^*(t) \quad (17)$$

$$i_q = W_a I_q^*(t) \quad (18)$$

$$I_c = i_d + i_q \quad (19)$$

Generating reference current, it is compared with the actual source current to generate gate pulse for the inverter. The compared signal is transferred through a hysteresis band to convert the signal to gate pulse. The modified control block diagram of the single-phase system is shown in Figure 2(b).

Simulation Results and Discussion

The overall system is simulated in MATLAB/Simulink software and the results are executed. Sample time of $10\mu s$ is considered for this simulation. PF in simulation is executed using the following equations (Cividino, 1992; Grady and Gilleskie, 1993).

$$\cos \phi = \cos(\theta_v - \theta_i) \times \sqrt{\frac{1}{1+THD^2}} \quad (20)$$

Where, θ_i and θ_v are the phase angle related to current and voltage respectively. Total harmonics distortion in terms of polluted rms current is,

$$THD = \frac{\sqrt{\sum_{k=2}^{\infty} I_{k rms}^2}}{I_{1 rms}} \quad (21)$$

The simulation diagram of power factor measurement subsystem is shown in Figure 3. The parameters considered for simulation is elaborated in Table 1. The DC-link capacitor of SAPF is charged to 326 V before connecting the SAPF to the system. This setting is done because of NLPID due to which the capacitor charge itself within very less amount of time results in drawing peak current from source. The SAPF was connected after 0.5 sec. to the system in simulation. Further

this section will discuss the results of non-linear loads and linear loads.

Table 1. SAPF and system parameters

System parameter	Value
Power	1 kW
Single phase source	230 V, 50 Hz
DC- link voltage	400V
Coupling Inductance (L)	$0.3\Omega, 6\text{ mH}$
DC-link capacitance (C_{DC})	$1250\text{ }\mu\text{F}$
α_1, α_2	0.8
K_{p1}, K_{p2}	0.32, 0.03
R_L, L_L	$5\Omega, 0.6\text{ mH}$
C_F, R_{DC}	$470\text{ }\mu\text{F}, 100\text{ }\Omega$
R_{LL}, L_{LL}	$26\Omega, 100\text{ mH}$

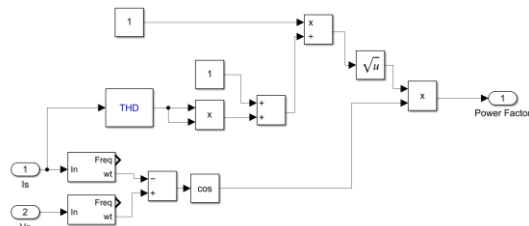


Figure 3. Power factor measurement subsystem

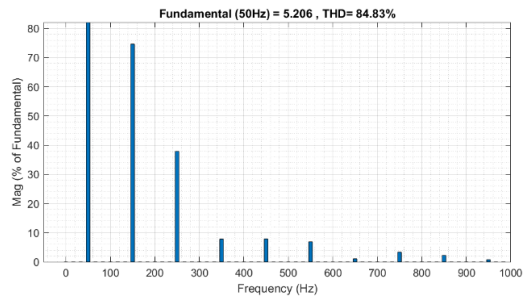


Figure 4. THD result of source current before compensation

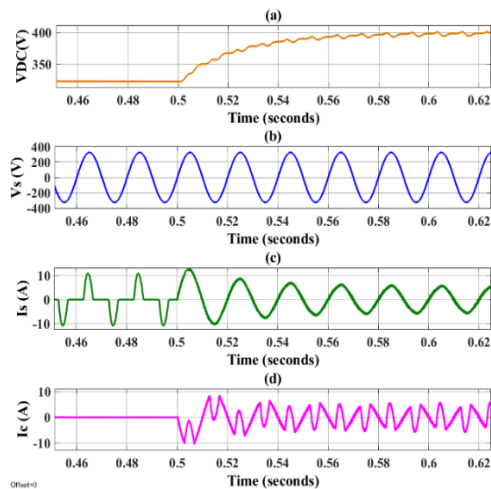


Figure 5. Results during non-linear load connected to the system (a) DC- link voltage, (b) source voltage, (c) source current and (d) compensating current of SAPF

A. Non-linear load

This subsection shows the results of the system when it was loaded with only non-linear load. Figure 4 shows the result of THD evaluation before compensation which is reported 84.83%. After SAPF was connected to the system the DC-link voltage of SAPF reached to 400 V as represented in Figure 5(a). The source voltage and current before and after compensation is shown in Figure 5(b) and Figure 5(c). The PF was 0.7592 which is improvised to 0.9952. The injected current from SAPF is represented in Figure 5(d). After compensation, the THD is reduced to 4.28 % as shown in Figure 6.

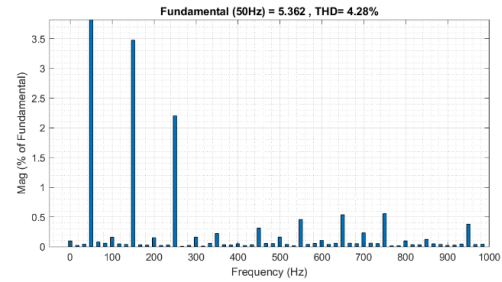


Figure 6. THD result of source current after compensation

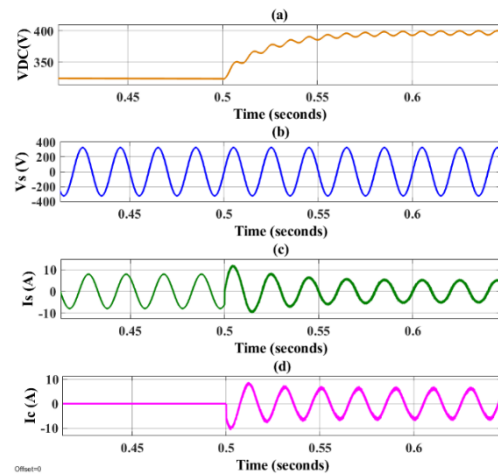


Figure 7. Results during linear load connected to the system (a) DC- link voltage, (b) source voltage, (c) source current and (d) compensating current of SAPF.

B. Linear load

The results of the system, when it was loaded with only linear load, is discussed in this subsection. The DC-link voltage, source voltage, and current before and after compensation can be observed in Figure 7. The PF was 0.6376 before connecting the SAPF to the system, after connecting the SAPF it is corrected to 0.9956. The voltage and current profile can be observed from Figure 7 (b and c). The compensation current is shown in Figure 7(d).

After compensation THD evaluation is represented in Figure 8. THD observed is 3.73% after SAPF connected to the system which is below 5% following the IEEE 519-2022 standard.

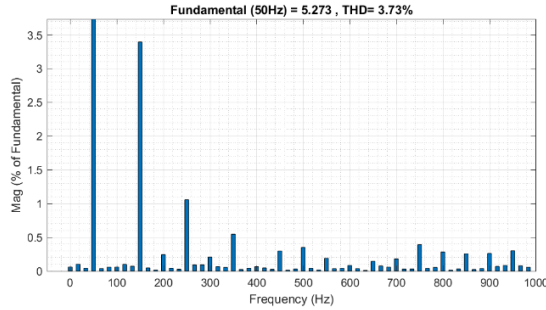


Figure 8. THD result of source current after compensation during linear load.

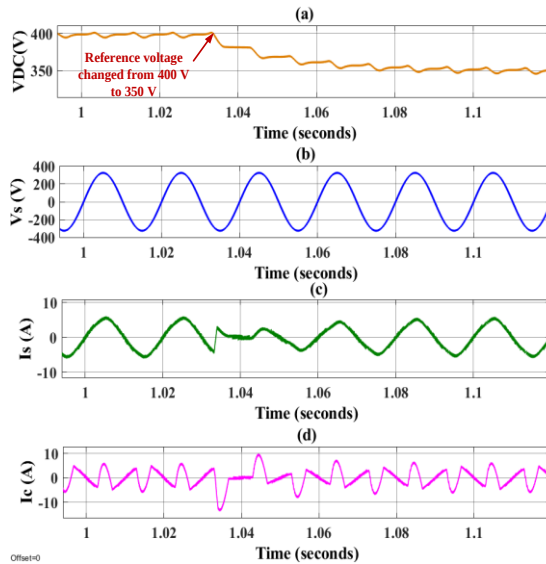


Figure 9. Results of DC reference voltage change

Overall, it is observed that for all types of loads the settling time of the DC-link voltage is 0.06 sec. which can be analysed from Figure 5(a), Figure 7(a). The system was also tested by changing the reference voltage of DC link voltage in the control system and the results are presented in Figure 9. It is noted that reducing the DC reference voltage to 350V from 400V doesn't affect the system. The settling time of the DC voltage is also the same as it was before. It is observed that the settling time of the DC voltage is between (0.06-0.08) sec., whereas the settling time of the source current is between (0.01-0.02) sec. All the simulated are summarised in a tabular form which is represented in Table 2. Also, after comparing the previous literature, it is found that this work can provide the lesser settling time of DC voltage of SAPF as represented in Table 3. So, this modified control

scheme can solve multiple power quality issues including reducing the settling time of the DC voltage.

Table 2. Result Summary

Load	SAPF status	PF	THD %
Non-linear load	Before compensation	0.7592	84.83
	After compensation	0.9952	4.28
Linear load	Before compensation	0.6376	0
	After compensation	0.9956	3.73

Table 3. Comparison Table

Ref.	Response time
Deffaf <i>et al.</i> , (2023)	0.13 sec.
Bajaj <i>et al.</i> , (2021)	(0.07- 0.5) sec.
Proposed scheme	0.06 sec.

Conclusion

A modified control scheme is proposed for single-phase SAPF. This control scheme is introduced for possible applications in remote areas where single-phase loads are prominent. The proposed control scheme has the capability to enhance the power factor and reduce the harmonic content of the power supply. Also, the proposed scheme can regulate and reduce the settling time of the DC link voltage of SAPF. The system is simulated in Matlab/ Simulink and found the settling time of the DC-link voltage is 0.06 sec.; the PF result is nearly to unity and the THD is below 8% which is within the limit of IEEE 519-2022 standard. These results indicate the scheme's suitability for rural and isolated areas, where maintaining power quality is often challenging, thereby supporting more stable and efficient electrical systems in such regions.

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