

# THE MODELLING AND ANALYSIS OF TEMPERATURE-DEPENDENT SILICON AND SILICON CARBIDE-BASED POWER DEVICE PERFORMANCE FOR HIGH-VOLTAGE APPLICATIONS USING MACHINE-LEARNING APPROACHES

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## Abstract

This study has revealed that On-State-Drain to Source resistance  $R_{DS(on)}$  is one of the most significant variables influencing the performance of silicon and SiC-based power semiconductor devices in high-voltage applications. The low  $R_{DS(on)}$  of power devices helps to drastically cut energy usage, enabling customers to create greener systems and products that lower CO<sub>2</sub> emissions. In SiC MOSFETs, low  $R_{DS(on)}$  enables significant system size and power consumption reductions in a range of applications, including traction inverters for electric vehicles and switching power supply. This work analyses the characteristics of silicon (Si) and Silicon Carbide (SiC)-based power semiconductor devices' performance in terms of total gate charge, drain current, power dissipation, thermal resistance and switching speed. This work affirms that SiC-based power devices provide superior performance as compared to silicon power devices for the abovementioned parameters at the same voltage rating of 650 V. The study highlights the effects of  $R_{DS(on)}$  on Si and SiC-based power devices and provides insight into the predictive modeling of the analyzed parameters at elevated temperatures, which is a novel contribution to this field of research. The models and formulations generated from this work help the designers select the power devices with the required  $R_{DS(on)}$  and correlate their effects by estimating the values of other important parameters, mainly, continuous drain current and zero voltage drain current at elevated temperature, with the exception of the real-time device testing procedure. The models and formulations generated using regression in this work are further validated using Mean Absolute Percentage Error (MAPE) and  $R^2$  techniques. The outcome of this work is expected to be implemented in the current machine-learning technology for device testing purposes.

**Keywords:** Silicon carbide; On-resistance; Temperature; Regression; Machine-learning

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## Introduction

Silicon carbide (SiC) device technology has emerged from research into commercial production and is regarded as one of the important materials for the next generation of high-voltage applications (Casady *et al.*, 1998; She *et al.*, 2017). When compared to silicon, SiC material performs better under high temperatures, high frequencies, and high voltages and has superior properties like low-loss semiconductors because of their low on-resistance (Glaser *et al.*, 2011; Cheng, 2018a). In addition, these prominent materials use fewer components, further reducing design complexity, particularly in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) which operate at extremely high voltages (Xuning and Gin, 2020). SiC has a 10 times higher dielectric breakdown intensity of the electric field than silicon, which enables it to reach a very high breakdown voltage, from 600V to a few thousand volts (Tsunenobu, 2022).

On the other hand, higher doping concentrations are used in SiC than in silicon, which helps the drift layers in SiC material be very thin (Casady *et al.*, 1998). The thinner the drift layer, the lower its resistance. When it comes to power devices, the high critical field strength can be leveraged to create switching components like Schottky barrier diodes and MOSFETs that operate at high voltages with considerably less loss and faster operation than typical silicon-based devices (Singh, 2006; Yuvraja *et al.*, 2023). In this work, a comparison study between silicon and SiC-based MOSFET at 650 V rating is performed in terms of electrical, dynamic, and thermal analysis.

The specific On-State-Drain to Source resistance  $R_{DS(on)}$  is the crucial parameter for power switches. The value of this parameter represents the total amount of resistive losses that a device produces when operating in forward conduction mode. In a range of high-voltage applications, including switching power supply and electric car traction inverters, low  $R_{DS(on)}$  power device ratings help significantly reduce system size and power consumption (Hren *et al.*, 2023). In this work, the effects of  $R_{DS(on)}$  values on power device electrical and dynamic parameters such as drain current and zero gate voltage current are analyzed in regard to elevated temperatures.

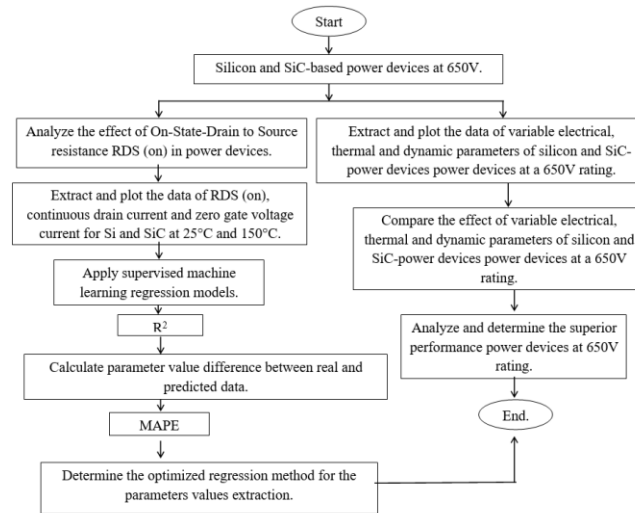
This work measures the relationship of  $R_{DS(on)}$  variations with the abovementioned parameters using supervised machine-learning techniques,

which include linear, polynomial and power curve regression. The models and formulations generated using regression in this work are further validated using Mean Absolute Percentage Error (MAPE) and  $R^2$  techniques. This work is intended to aid the designers in selecting the power devices, taking into account  $R_{DS(on)}$  values and correlating their effects by estimating the values of other important device parameters which, mainly focus on continuous drain current and zero voltage drain current at elevated temperatures with the exception of the real-time device testing procedure. In this study, it will greatly decrease the time, costs, and resources required for processing. As the technology of machine learning advances, the insights made in this research can be integrated into the tools used for semiconductor production.

## Materials and Methods

Figure 1 shows the flowchart of the methods carried out to perform analysis on the silicon and SiC MOSFET at 650 V. The charts present the method to formulate the effect of  $R_{DS(on)}$  in relation to power devices' electrical parameters at elevated temperatures of 25°C and 150°C. On the first level, four samples of power devices, mainly MOSFET fabricated using silicon and SiC, were selected from Infineon's manufacturing datasheet. The voltage rating for selected samples is 650 V, coupled with various  $R_{DS(on)}$  values. By using the datasheet, the key parameters associated with  $R_{DS(on)}$  are extracted, which include electrical, dynamic, and thermal-based parameters and further analyzed. This is followed by extracting and plotting the data of  $R_{DS(on)}$ , drain current and zero gate voltage current for Si and SiC at 25°C and 150°C. Then, a systematic investigation of the  $R_{DS(on)}$  effect relationship with the extracted parameters is presented.

Predictive analytics is used to estimate and forecast future events by employing a variety of statistical approaches, such as machine learning, predictive modeling, and data mining (Balen *et al.*, 2022). Predictive analytics technology assists in comprehending potential future events by analyzing the past. Techniques that are widely used include the following:



**Figure 1. Flowchart of the methods carried out to perform analysis on the silicon and SiC MOSFET at 650 V.**

- i. Decision trees: The techniques employ open-source data to graph it out in branches to show the likely outcomes of various options. Decision trees use previous judgments to describe response components and forecast response variables (Charbuty and Abdulazeez, 2021).
- ii. Time series analysis: This technique predicts occurrences that occur over time. By evaluating prior trends, it is possible to predict future trends. A time series is an ordered number of data points gathered at certain intervals of time that are unable to dispersed equally apart or may contain data gaps, resulting in inconsistent spacing or an unevenly sampled time series. The irregular noise-induced errors may lead to results being weighted unfairly in some cases (Ghaderpour *et al.*, 2021).
- iii. Logistic regression is a mathematical analysis method for projecting a data value based on historical data set observations. The predictions are generated as more data is added and the algorithm improves at sorting and classifying the data (Chukhrova and Johannssen, 2019).
- iv. Neural networks: a method for examining large amounts of labeled data to find correlations between the variables in the data. This approach is used to build artificial intelligence (AI), which includes natural language interpretation, smart assistants, and image recognition (Bau *et al.*, 2020).

These several prediction analytics approaches are used according to the benefits of each model and how each one may be improved by various predictive analytics algorithms (Junta *et al.*, 2022). The analysis of the variables that determine whether

an intervention will result in improvement or failure is one of the uses of prediction analytics in machine learning.

One of the supervised machine-learning techniques is regression methods (Maulud and Abdulazeez, 2020; Kurama, 2023). Specifically, linear, polynomial and power curve regressions are used to determine the estimated  $RDS_{(on)}$  with various parameters. A linear regression line has the formula  $Y = a + bX$ , where  $X$  is the variable that explicates the equation, while  $Y$  is a variable that is dependent.  $A$  is the interception (the value that corresponds to  $y$  when  $x = 0$ ), and  $b$  is the gradient of the line. Polynomial regression, which uses an equation of the type  $Y = 0 + 1X + 2X^2 + \dots + hX^h$ , where  $h$  is referred to as the degree of the polynomial, is used to model the nonlinear relationship between  $X$  and  $Y$ . There is a designated name for relationships with lower degrees (e.g.,  $h = 2$  is referred to as quadratic,  $h = 3$  is referred to as cubic,  $h = 4$  is referred to as quartic, and so on) (Norman and Harry, 1998; Cheng *et al.*, 2018b). For power curve regression, the logarithm of both sides of the equation  $y = axb$  is taken, which transforms to  $Y = \log y = \log(axb) = \log a + b \log x = \alpha + \beta X$ . To compute manually, the logarithm of both  $x$  and  $y$  is taken, thus, the model transformation represents  $Y = \log y$  and  $X = \log x$ .

Referring to Figure 1, the models and formulations generated from this work are further validated using the  $R^2$  and Mean Absolute Percentage Error (MAPE) approaches. Based on the graphs, the regression method is used to fit the points and obtain the models for the  $RDS_{(on)}$  values. Using the models, the parameter values are further determined. A statistical measure representing the

proportion of a regression model's dependent variable's variance can be accounted for by the independent variable or variables (Chicco *et al.*, 2021; Myttenaere *et al.*, 2015). The expression (1) presents the formula for  $R^2$ .

$$R^2 = 1 - \frac{RSS}{TSS} \quad (1)$$

$R^2$  = determination of coefficients  
 RSS= total squares of the residuals  
 TSS = sum of the squares total

MAPE is the average of the percentage errors (Myttenaere *et al.*, 2015) as per Expression (2).

$$MAPE = \frac{\sum_{t=1}^n \left( \frac{|X_t - \hat{X}_t|}{X_t} \right)}{n} \times 100\% \quad (2)$$

$n$  is the total amount of fitting points,

$X_t$  is the original value,

$\hat{X}$  is the predicted value.

$\Sigma$  is the summation notation which comprises the accumulation of the absolute value for each predicted time point.

$R^2$  coefficient is used to analyze the relationship between  $RDS_{(on)}$  and various device parameters. The accuracy of the models that describe the discrepancy between real and forecasted values is further validated using MAPE.

The primary objective of this work is to investigate the effect of  $RDS_{(on)}$  on SiC-based device performance and develop a formulation for  $RDS_{(on)}$  towards device parameters for high-power applications at 650 V. With the developed predictive modelling methods, the values of device parameters could be determined with various degrees of accuracy, with the exception of real-time device testing procedures. The results are expected to be integrated into the upcoming machine-learning technology.

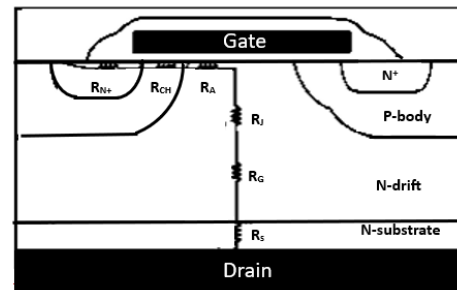
On the other hand, a comparison of the effects of variable electrical, thermal, and dynamic parameters on silicon and SiC-power devices at a 650 V rating is presented in this work.

The analyzed parameters include continuous drain current, total gate charge, power dissipation, and thermal resistance junction-case. Then, the analysis and determination of the superior performance power devices at 650 V are presented (Figure 1).

## Results and Discussion

Figure 2 shows the vertical layout of a MOSFET as well as the series of resistances that altogether make

up the sum of  $RDS_{(on)}$  along the current flow route from source to drain. When the switch is turned on, a number of resistances along the way from source to drain are present. These resistances together are named as  $RDS_{(on)}$ , which is a representation of the total resistance along that path. The diffusion resistance of the source region is denoted by  $R_N$ .  $R_{CH}$  stands for the resistance of the channel region. The accumulation region's resistance is denoted by the abbreviation  $R_A$ . The JFET region's resistance is denoted by the letter  $R_J$ . The most crucial element in high-voltage MOSFETs is called the drift region resistance ( $R_D$ ).  $R_S$  stands for the substrate's own resistance (Semiconductor Component Industries, 2000; Saavedra-Gómez *et al.*, 2023; Rohm Semiconductor, 2023).



**Figure 2.** The figure shows the vertical layout of a MOSFET as well as the series of resistances that together make up the total  $RDS_{(on)}$  in the current flow route from source to drain

Besides these intrinsic structural causes of  $RDS_{(on)}$ , other factors that might cause  $RDS_{(on)}$  include faulty source-drain metal contact and even wire that links the die to the package's leads. The latter is denoted by the  $R_{WCML}$ , which is the sum of the contact resistance, bond wire resistance and lead frame resistance (Abhijit, 2011). The on-resistance often reduces as the  $V_{GS}$  rises. When a particular  $V_{GS}$  is used,  $RDS_{(on)}$  occurs. The MOSFET's on-resistance should be as low as possible since low resistance lowers unwanted power dissipation and increases the device's power efficiency (Teknonix, 2023).

Furthermore, reducing  $RDS_{(on)}$  is critical for high-power devices since it lowers switching losses, enhances breakdown voltages, and provides higher temperature capability. These provide power-conversion system designers more flexibility to improve energy efficiency, specify smaller components, and streamline thermal management to reduce size and engineering costs without compromising dependability.

$RDS_{(on)}$  rises as temperature rises (also referred to as a positive temperature coefficient). This is due to the fact that when the temperature rises, the mobility of the hole and electron decreases. The following Expression (3) (Semiconductor Component Industries, 2000) states that  $RDS_{(on)}$  is a function of temperature:

Figure 3 shows the relationship between  $RDS_{(on)}$  and power devices, which are silicon-based MOSFET and SiC-based MOSFET at 650 V, respectively. The plots in Figure 3 show that  $RDS_{(on)}$  for 150°C is higher than 25°C which agrees with the statement as temperature increases,  $RDS_{(on)}$  increases accordingly. Based on Figure 4, it is noticed that the increment of  $RDS_{(on)}$  in silicon-based MOSFET is higher than in SiC-based

MOSFET. This clearly demonstrates the advantage of SiC MOSFET which have the capability to withstand high-temperature conditions as compared to their silicon counterparts. Generally, at high temperatures, the  $RDS_{(on)}$  of the high breakdown voltage of Si MOSFET increases dramatically. The drift layer resistance (RD), which makes up 90% or more of a device's on-resistance, tends to increase by around two times when the temperature is raised by 100°C as one possible explanation for this increase (Vishay Siliconx, 2016). Based on the  $R^2$  values in Figure 3, the polynomial regression method provides optimum fitting with the highest  $R^2$  and least MAPE for silicon and SiC MOSFETs, respectively.

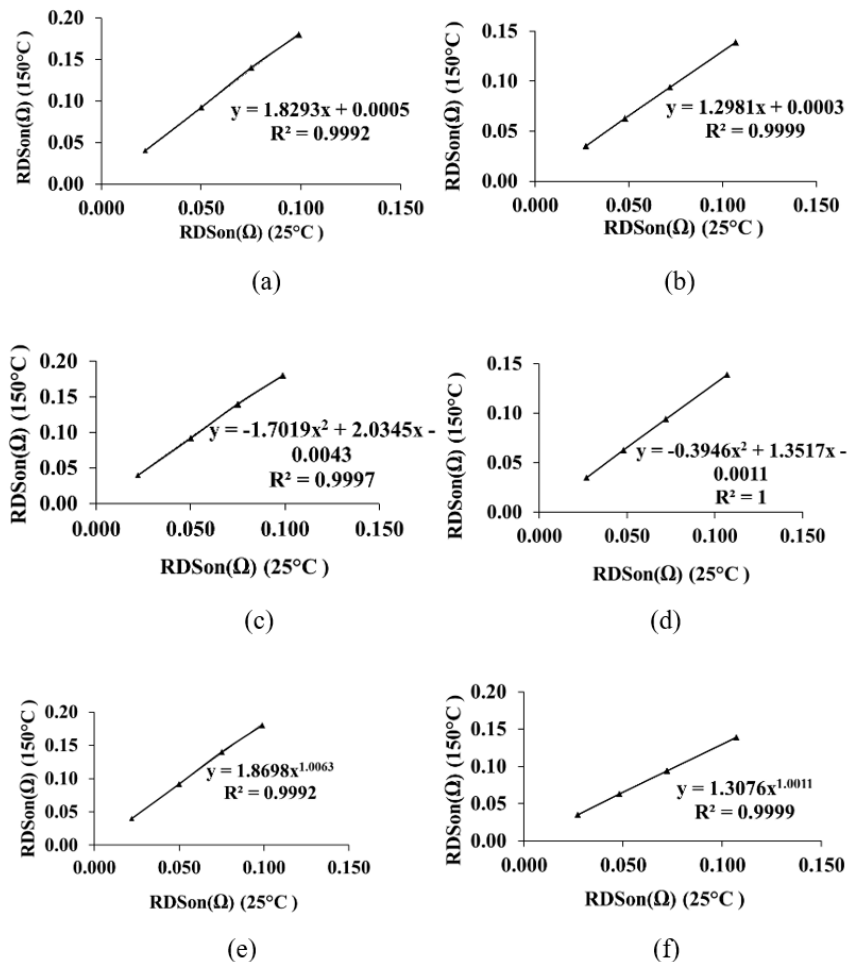


Figure 3. Plots show the relationship between the  $RDS_{(on)}$  of power devices that are silicon-based MOSFETs and SiC-based MOSFETs at 650 V: (a) linear regression (silicon); (b) linear regression (SiC); (c) polynomial regression (silicon); (d) polynomial regression (SiC). (e) power regression (silicon) (f) power regression (SiC)

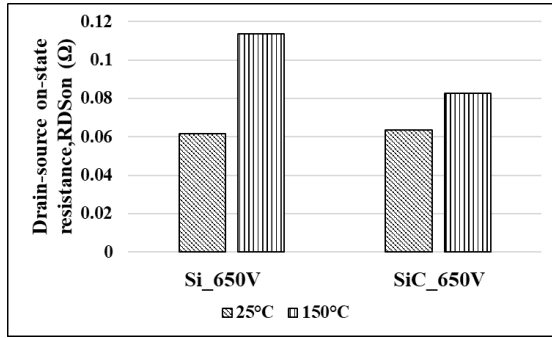


Figure 4. Graphs show the comparison results of  $R_{DS(on)}$  at elevated temperatures of 25°C and 150°C for silicon and SiC at 650V, respectively

Another important parameter is the continuous drain current. The plots in Figure 5 show that the continuous drain current for 150°C is lower than 25°C. It can be seen that as the  $R_{DS(on)}$  increases, the drain current decreases, which is justified by Ohm's Law ( $V=IR$ ). Based on Figure 6, it is noticed that the decrement of drain current in a silicon-based MOSFET is higher than in a SiC-based MOSFET. This clearly demonstrates the advantage of SiC MOSFETs, which have the capability to provide a more stable drain current regardless of high-temperature conditions as compared to their silicon MOSFET counterparts. Based on the  $R^2$  values in Figure 5, the power regression method provides optimum fitting with the highest  $R^2$  and least MAPE for silicon and SiC MOSFETs, respectively.

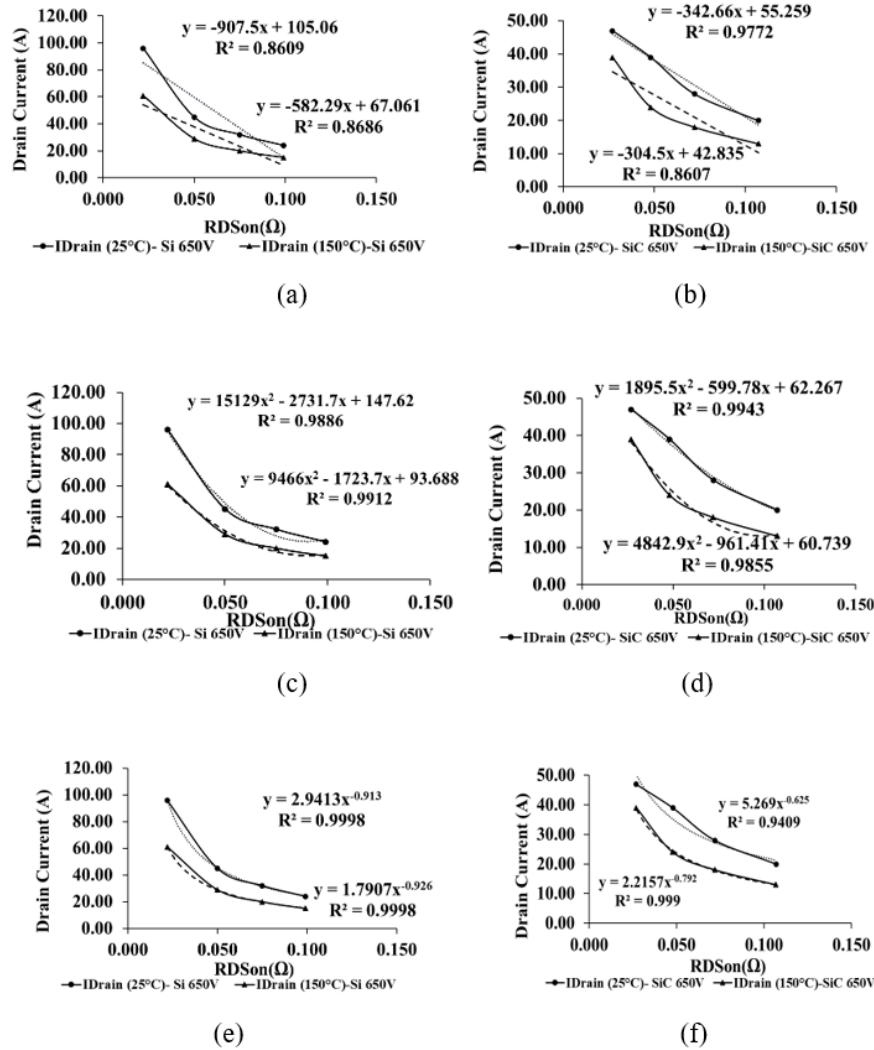
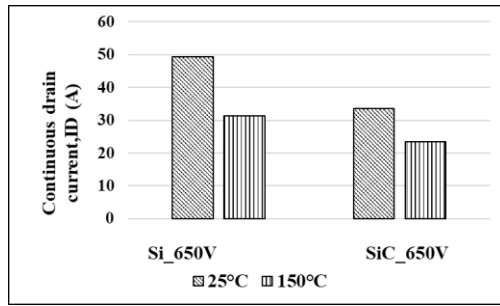


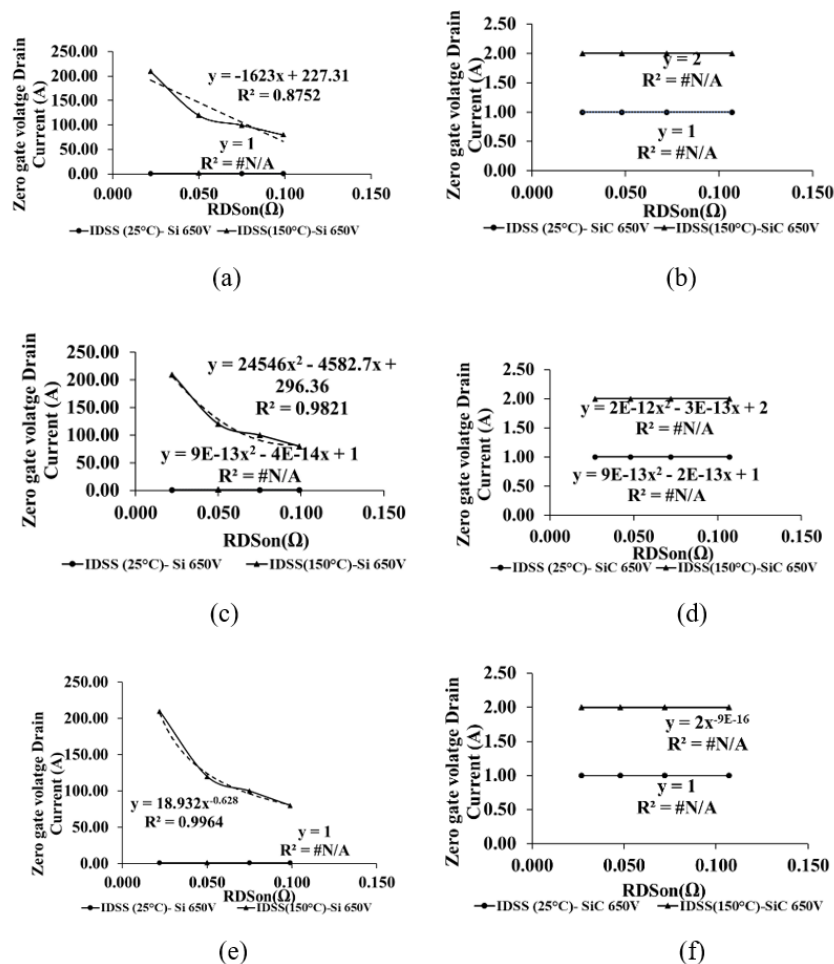
Figure 5. Plots show the relationship between drain current and  $R_{DS(on)}$  for silicon and SiC-based MOSFETs at 650 V (a) linear regression (silicon); (b) linear regression (SiC); (c) polynomial regression (silicon); (d) polynomial regression (SiC) (e) power regression (silicon) (f) power regression (SiC)



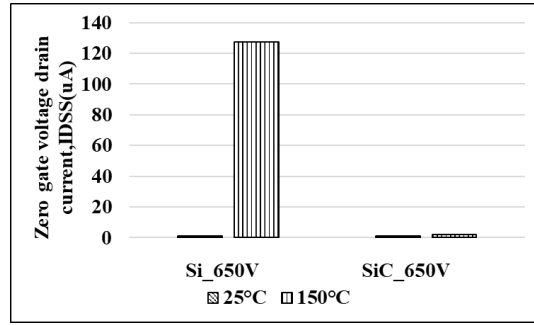
**Figure 6.** Graphs show the comparison results of drain current at elevated temperatures of 25°C and 150°C for silicon and SiC at 650V, respectively

Figure 7 shows the relationship between zero gate voltage drain (IDSS) and  $R_{DS(on)}$  for 650V

silicon and silicon carbide MOSFETs. Zero gate voltage drain current is the flow of current when  $V_{GS}=0$ . It shows that the drain leakage current decreases as the  $R_{DS(on)}$  increases for the Si 150°C MOSFET. However, the drain current leakage is constant for silicon at 25°C and SiC at 25°C and 150°C. Figure 8 shows that the  $ID_{SS}$  tends to increase at a higher temperature; the increment is more obvious for silicon MOSFET than SiC at 650V rating. This clearly demonstrates the advantage of SiC MOSFETs, which have the capability to provide less leakage current regardless of high-temperature conditions as compared to their silicon MOSFET counterparts. Based on the values in Figure 7, the power regression method provides optimum fitting with the highest  $R^2$  and least MAPE for silicon and polynomial regression for SiC MOSFETs, respectively.



**Figure 7.** Plots show the relationship between the zero gate voltage drain current of power devices and the respective  $R_{DS(on)}$  for silicon and SiC-based MOSFETs at 650 V (a) linear regression (silicon) (b) linear regression (SiC) (c) polynomial regression (silicon) (d) polynomial regression (SiC) (e) power regression (silicon) (f) power regression (SiC)



**Figure 8. Graphs show the comparison results of zero gate voltage drain current at elevated temperatures of 25°C and 150°C for silicon and SiC at 650V, respectively**

Table 1 presents the summary of results showing the optimized techniques, model formula,  $R^2$  and MAPE for silicon and SiC MOSFETs at 650 V.

In Figure 9, the relationship between the total gate charge for silicon and SiC MOSFETs operating at 650V is presented. The total gate charge denotes the quantity of charge required to drive (turn ON) the MOSFET<sup>21</sup>. The total gate charge ( $Q_g$ ), measured in Coulombs (C), is a measure of the time it takes to charge the capacitor needed to turn on a MOSFET, which raises switching loss. However,

if this value is lower, switching loss will be reduced and switching speed will be faster. This can be clearly seen in Figure 10(a) and (b) as silicon MOSFET have a higher turn-on and turn-off delay time, which contributes to higher switching losses compared to their SiC counterparts.

The comparison of power dissipation for silicon and SiC at 650V at increased temperatures of 25°C and 150°C is shown in Figure 11. The power dissipation of the MOSFET is directly proportional to the chip size of the device (Li *et al.*, 2017). A MOSFET experiences power dissipation when the drain current and drain-source voltage are both greater than zero. The maximum amount of power that a MOSFET can continuously dissipate under certain temperature conditions is known as power dissipation. It is observed that the power dissipation for SiC MOSFETs is lower than for silicon MOSFETs.

Another important parameter is the thermal resistance, junction-case. When thermal resistance in the junction-case is low, heat conduction is increased, and when it is high, heat conduction is lowered. Junction-to-case thermal resistance ( $\theta_{JC}$ ) is defined by the following expression (4) (Li *et al.*, 2017):

$$\theta_{JC} = \frac{T_J - T_C}{P_D} \quad (4)$$

**Table 1. Summary of results showing the optimized techniques, model formula,  $R^2$  and MAPE for (a)silicon and (b)SiC MOSFETs at 650 V.**

| Technology     | Parameters                                    | Model Formula                  | Method     | $R^2$  | MAPE(%) |
|----------------|-----------------------------------------------|--------------------------------|------------|--------|---------|
| Silicon (650V) | Drain-source on-state resistance (Dron)@150°C | $y = -1.7019x2.0345x - 0.0043$ | polynomial | 0.9997 | 0       |
|                | Drain Current(A)@25°C                         | $y = 2.9413x - 0.913$          | power      | 0.9998 | 1.06    |
|                | Drain Current(A)@150°C                        | $y = 1.7907x - 0.927$          | power      | 0.9998 | 1.08    |
|                | Zero gate voltage drain current@25°C          | $y = 1$                        | power      | N/A    | 0       |
|                | Zero gate voltage drain current@150°C         | $y = 18.932x - 0.628$          | power      | 0.9964 | 2.32    |

(a)

| Technology             | Parameters                                     | Model Formula                      | Method     | $R^2$  | MAPE(%) |
|------------------------|------------------------------------------------|------------------------------------|------------|--------|---------|
| Silicon Carbide (650V) | Drain-source on-state resistance (RDSon)@150°C | $y = -0.3946x2 + 1.3517x - 0.0011$ | polynomial | 1.000  | 0       |
|                        | Drain Current(A)@25°C                          | $y = 1895.5x2 - 599.78x + 62.267$  | polynomial | 0.9943 | 2.05    |
|                        | Drain Current(A)@150°C                         | $y = 2.2157x - 0.792$              | power      | 0.9990 | 1.03    |
|                        | Zero gate voltage drain current@25°C           | $y = 1$                            | power      | N/A    | 0       |
|                        | Zero gate voltage drain current@150°C          | $y = 2x - 9E-16$                   | power      | N/A    | 0       |

(b)

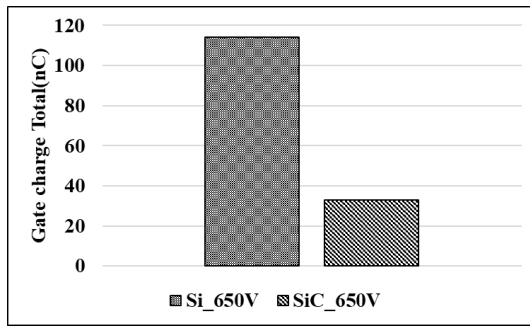
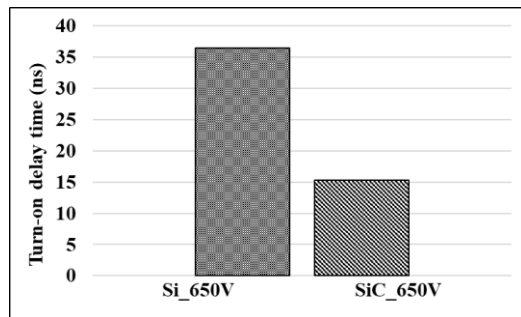
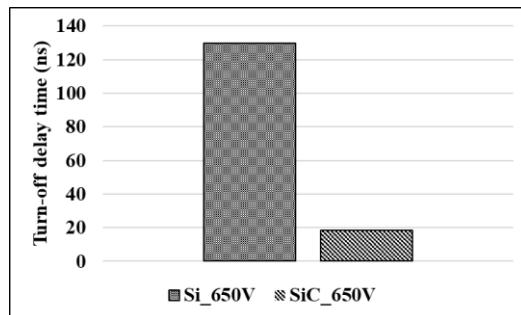


Figure 9. Graphs show the comparison results of total gate charge at elevated temperatures of 25°C and 150°C for silicon and SiC at 650V, respectively



(a)



(b)

Figure 10. Graphs show the comparison results of (a) turn-on delay time (b) turn-off delay time at elevated temperatures of 25°C and 150°C for silicon and SiC at 650V, respectively.

Where  $T_j$  is the semiconductor device junction temperature (°C),  $T_c$  is the external case or package temperature (°C), and  $P_D$  is the power dissipation (Watts). According to the equation above, the  $\theta_{JC}$  parameter is expressed in terms of degrees Celsius per Watt (°C/W). Figure 12 shows that SiC MOSFET has a higher thermal resistance than Si MOSFET. The results are in agreement, as  $P_D$  is inversely proportional to  $\theta_{JC}$ . This is further

evidenced as SiC MOSFETs dissipate less power than silicon MOSFETs, as shown in Figure 11.

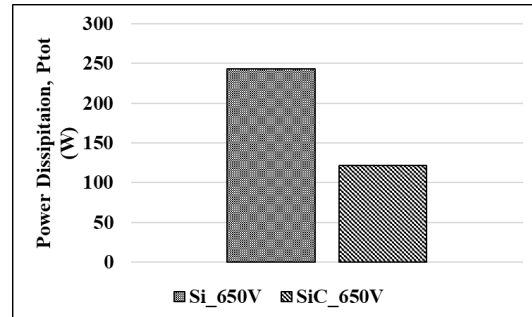


Figure 11. Graphs show the comparison results of power dissipation at elevated temperatures of 25°C and 150°C for silicon and SiC at 650V, respectively

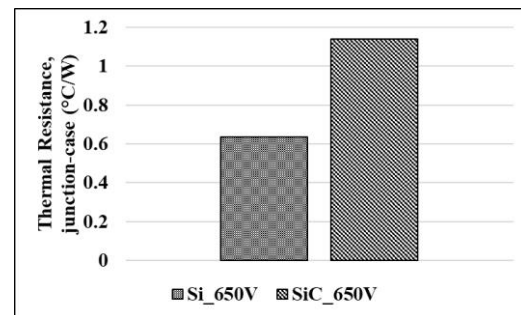


Figure 12. Graphs show the comparison results of thermal resistance, junction-case at elevated temperatures of 25°C and 150°C for silicon and SiC at 650V, respectively

## Conclusions

This work evaluates silicon and SiC MOSFET performance based on varied  $R_{DS(on)}$ , mainly for high voltage applications at 650V. The outcome of this work revealed that SiC MOSFETs provide superior performance in terms of power dissipation, thermal resistance, and switching speed as compared to silicon power devices at the same voltage rating of 650 V. The relationship between the drain and zero gate voltage drain current is determined using linear, polynomial, and power regression methods and further validated using  $R^2$  and MAPE. As compared to linear and polynomial regression, it is noticed that polynomial regression provides better fitting accuracy for  $R_{DS(on)}$  at 25°C versus 150°C for both silicon and SiC MOSFETs and SiC MOSFET drain current at 25°C. On the

other hand, power curve regression is well suited for the rest of the parameter studies for silicon and SiC MOSFETs at 25°C and 150°C, respectively. The MAPE and  $R^2$  for power curve regression are below 3% and above 0.9, respectively, indicating a strong relationship between  $R_{DS(on)}$  and drain current and zero gate voltage drain current. Based on the obtained results, formulations have been developed that function as predictive models for the device parameters at selected  $R_{DS(on)}$  values. The outcome of the study revealed that  $R_{DS(on)}$  plays a vital role, particularly at elevated temperatures, in device performance aspects for high-power device applications. The models and formulations generated from this work are expected to aid the researchers in providing a brief overview of the device performance associated with varied  $R_{DS(on)}$ . In conjunction with the advancement of technology in the semiconductor sector, the output of this work can be applied in a machine-learning context. Hence, this work enables the reduction of processing time, material, and cost, with the exception of expensive device testing work for SiC-based power devices, which are mainly used in high-power applications.

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