

GEOMETRIC INVESTIGATION AND PERFORMANCE ANALYSIS OF SOI FINFET FOR RF/AF PARAMETERS

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Abstract

FinFET-based devices provide better and faster operational performance and, thus, are widely preferred to be integrated into a complex circuit application. The present paper has proposed a silicon on insulator (SOI) FinFET and studies the effect of h_{fin} variations (1.3, 1.0, 0.7, 0.25) and W_{fin} variations (1.0, 0.6, 0.25) on structure performance metrics, counting low-frequency limitations such as transconductance (G_m), output conductance (G_d), capacitances and voltage gain (A_v). The structure clearly shows excellent efficiency for (i) $h_{fin}/L_g = 0.7$ figure by increasing device gain and operational frequency; (ii) $W_{fin}/L_g = 0.6$ figure by optimizing structure intrinsic resistance, A_v , and VEA, thereby making the device perform without even any substrate impact, according to simulations conducted using the SILVACO tool. The investigation has identified that structure length variation could provide varied performances, such as higher device-current being recommended for improved current drivability and smaller devices being preferred for reducing SCEs and increasing device immunization. The current study can serve as a starting point for 3-D device simulators looking to attain improved performance.

Keywords: Terms-Silicon On Insulator (SOI), Radio Frequency (RF), TCAD tool, FinFET, Voltage Gain.

Introduction

Conventional MOSFETs have a lot of parasitic capacitance, latch-up, short channel effects (SCEs), and surface mobility deterioration due to direct scaling. The relationship of scaling measures to the reduced size of MOSFETs has enabled complementary MOS (CMOS) innovation [1-5]. The switching speed and density of the device have improved as a result of the nanometer-scale design. Resolving distinct concerns such as increased spilled current raises the temperature in CMOS-based devices [6] but makes the device considerably more complicated. Dual Gate (DG) MOSFETs are another alternative for designing SCE-free devices with a greater ON current and improved sub-threshold slope [7]. A simulation of a DG-MOSFET found that it has a higher drive current, less band-to-band tunneling, and lower parasitic capacitance, making it ideal for digital logic circuits. But, misalignment causes excess gate-to-source/drain

capacitance and resistance, therefore aligning both gates in symmetry is a problem. Another contender is the Silicon-on-Insulator (SOI) MOSFET, which has very low SCEs at desired latch-up when SOI is much reduced at source/channel. or by the use of back-entryway predisposition. However, the floating body effects, low transport efficiency, unfulfilled breakdown, and self-healing effects device performance [8]. A self-aligned FinFET structure is provided to overcome the difficulties stated with DG-MOSFET devices. The FinFETs based on SOI technologies have a higher saturation current, lower leakage current, improved subthreshold properties, and low parasitic effects [9]. Compared to silicon-on-insulator (SOI) FinFETs, junctionless FinFETs provide more freedom in determining device characteristics, reducing the impact of SCEs [10-12]. FinFET structures are generally chosen in this form because

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of their reduced size, which allows for more hierarchy levels of functionality at high energy efficiency. It is critical to simulate discrete level devices for evaluating device performance variance in terms of application in the AF/RF circuit domain [13], [14]. The multigate FinFET device outperforms all other FinFETs in logic, packing density with analog/RF, and mixed-signal circuit performance. As a result, Silicon on Insulator (SOI) FinFET is proposed in the present work and geometrically evaluated for efficient RF/AF analysis.

The dynamical threshold (D_T) body is electrically coupled to the device gate terminal to boost on-state current (I_{ON}) without compromising the OFF-state (I_{OFF}) [13-15]. For a considerable increase in I_{ON} as well as other electrical performance in DT-mode bulk FinFETs, the width parameter W_{fin} must be large ($> 100\text{nm}$). Indeed, the W_{fin}/h_{fin} [16-18] is the most important setting in FinFET because it categorizes the device as (i) Finfet $W_{fin}/h_{fin} < 1$, tri-gate $W_{fin}/h_{fin} = 1$, or planar $W_{fin}/h_{fin} > 1$ (ii) maintains the trade-off among device performance and ratio because heightened devices have greater I_{ON} while short-length originates short channel impacts.

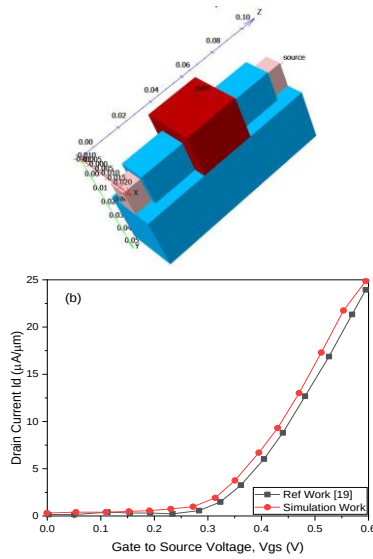


Figure 1. (a) Cross-sectional view of 3-D Silicon on Insulator FinFET structure (b) experimented drain outcomes [19].

Table 1. h_{fin} and W_{fin} ranges of 3D soi-fineet for simulation

S. No.	Device Parameters	Values
1	h_{fin}/L_g	1.3,1.0,0.7,0.25
2	W_{fin}/L_g	1.0,0.6,0.25

Device Design and Structure

Figure 1 depicts the simulation of a 3-D SOI FinFET in this paper. The structure parameters associated with design and modeling are mentioned here. An n-channel FinFET is designed with SiO_2 as an interfacial oxide layer. Other structure values used in the simulation are: ratio of source/drain length= 40 nm, doping density $N_D = 10^{20} \text{ cm}^{-3}$, supply voltage (V_{dd}) is 0.5 V, gate work function=4.65 eV.

Simulation Software: The simulation of the FinFET structure is conceded out in ATLAS TCAD software. Other physical models include, for example, non-local B2B (band to band) tunneling, Fermi-Dirac, Drift diffusion model, and velocity saturation were also utilized. To acquire V_{th} , different changes were performed to the values of metal gate work functions of the proposed structure.

The Table 1. summarises the instances used in the current work, which are based on a variety of h_{fin} and W_{fin} values.

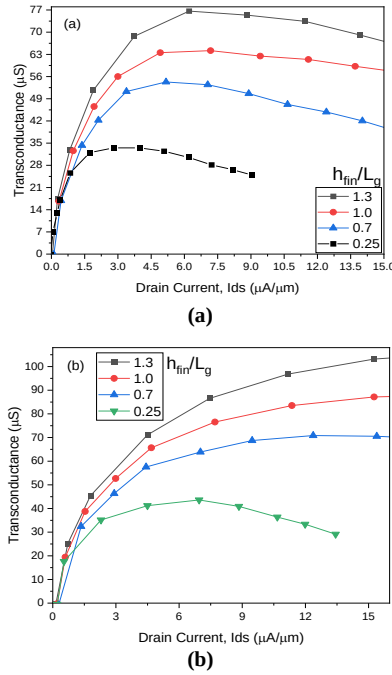
Results and Discussion

The behavior of the proposed FinFET device is investigated using low-frequency factors such as transconductance g_m , Output conductance g_d , Gate capacitance C_{gg} , and structure voltage gain A_v . The factors also investigated the operation of the proposed device in terms of h_{fin} and W_{fin} values.

A. Impact of h_{fin} :

As illustrated in Figures 3, 4, 5, and 6, the sensitivity change in h_{fin} upon various important device parameters is investigated. Figure 3 shows the transconductance g_m as a function of the device I_{ds} at $V_{ds} = 0.050 \text{ v}$ and 0.50 v and $L_g = 22 \text{ nm}$. The g_m versus I_{ds} curve suggested that as the h_{fin}/L_g ratio rises, the transconductance (g_m) and drain current (I_{ds}) parameters increase. At $h_{fin}/L_g = 1.1$ and $W_{fin}/L_g = 1.0$, the optimal values of I_{ds} and g_m were obtained.

The relation of output conductance g_d with V_{ds} for V_{gs} equal to a higher voltage (0.50 V) as well as lower voltage (50 mV) at various values of h_{fin}/L_g is investigated and presented in Figure 3. The enfolded gate provided a short FinFET structure $W_f/h_f < 1$ that displayed additional electrostatic control over the channel when it was fully depleted. The minimized channel length modulation and drain-bias dependency [20] results in a reduction in g_d by minimizing variance in I_d .



Not mentioned in the article.

Figure 2. Id-Vgs characteristics of the DMG-SOI FinFET for variable drain voltage a) 0.05 V and b) 0.50 V at $L_g=22$ nm, $W_{fin}=10$ nm, $t_{ox}=0.9$ nm, $t_{box}=40$ nm and $t_{sub}=75$ nm

The proposed structure gain g_m/g_d decreases as the value of g_d and h_{fin}/L_g ratio rises. The higher value of g_d and lower resistance results in a rise in the $I_d - V_{ds}$ particularly in the saturation zone. The curve of g_m/g_d with V_{gs} demonstrates that at various h_{fin}/L_g values, a rise in g_m/g_d value is observed at lower h_{fin}/L_g values, which gradually decreases with rising h_{fin}/L_g values. The reason for this is that as the h_{fin}/L_g ratio rises, the I_D rises as well.

The minimized channel length modulation and drain-bias dependency [21], results in a reduction in g_d and I_D variance.

The g_m of FinFET determines amplifier gain as shown in Equation (1). An improvement in g_m gives the higher carrier transport efficiency for the proposed structure that essential for analog applications.

$$g_m = \partial I_d / \partial V_{gs} \quad (1)$$

In Fig. 3, the output conductance (g_d) vs drain voltage at different values of $V_{ds}=0.05$ and 0.5 V are presented. For computing output conductance g_d , formula in Equation (2), is utilized.

$$g_d = \partial I_d / \partial V_{ds} \quad (2)$$

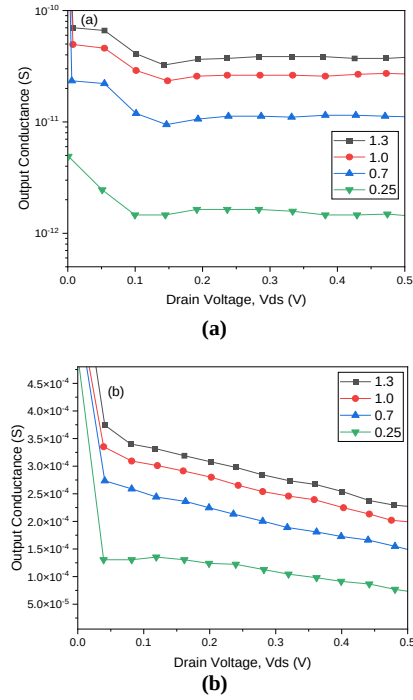


Figure 3. Curve for drain conductance (g_d) vs drain voltage V_{ds} at a) $V_{gs}=0.05$ V and. b) $V_{gs}=0.50$ V for $L_g=22$ nm, $W_{fin}=10$ nm, $t_{ox}=0.9$ nm, $t_{box}=40$ nm, $t_{sub}=75$ nm, with $V_{ds}: 0$ V-to-0.5 V

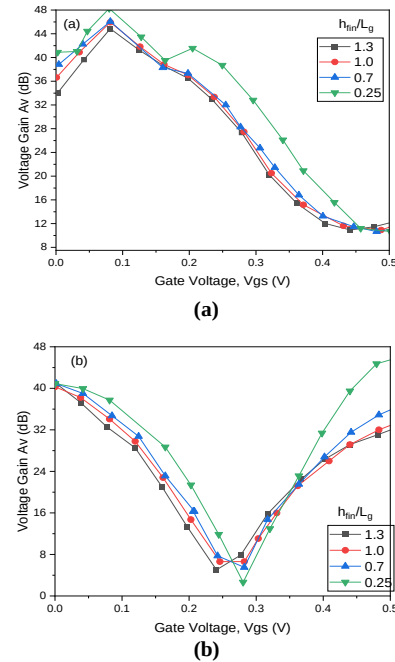


Figure 4. Proposed structure voltage gain $A_v = g_m/g_d$ Vs. gate voltage V_{gs} at variable drain voltage a) $V_{ds}=0.05$ V and, b) $V_{ds}=0.50$ V with $L_g=22$ nm, $W_{fin}=10$ nm, $t_{ox}=0.9$ nm, $t_{box}=40$ nm, $t_{sub}=75$ nm, $V_{gs}=0$ V-to-0.5 V.

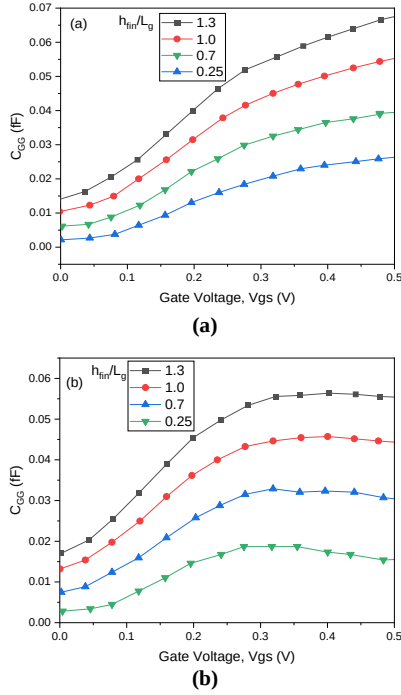


Figure 5. Proposed structure gate capacitance C_{gg} - V_{gs} at variable drain voltage a) $V_{ds}=0.05$ V and b) $V_{ds}=0.50$ V for $L_g=22$ nm, $W_{fin}=10$ nm, $t_{ox}=0.9$ nm, $t_{box}=40$ nm, $t_{sub}=75$ nm, with V_{gs} : 0 V-to-0.5 V

Figure 3(a) and Figure 3(b) depict output conductance g_d with V_{ds} for various FinFET regions and h_{fin}/L_g . As demonstrated in Fig. 4 (a and b), a decrease in the h_{fin}/L_g ratio resulted in a rise in voltage gain, which was driven by lower g_d values at lower h_{fin}/L_g values [22]. The g_m/I_{ds} factor shows how to use the current parameter to reach effectively g_m value that the device requires. A larger g_m/I_{ds} ratio is necessary for analog circuits that can operate at low supply voltages. A fluctuation in the ratio g_m/I_{ds} is found in the sub-threshold and inversion regions (i.e., at low values of V_{ds} and V_{gs}), [22], [23].

The fluctuation of C_{gg} at various values of V_{gs} of the structure is illustrated in Fig. 5 (a and b), with an increment in C_{gg} with rising h_{fin}/L_g ratio for the device. For h_{fin}/L_g levels, it is caused by an increase in the fringing field density. It is also discovered that $h_{fin}/L_g = 0.7$ confers significantly greater SCE immunity; thus, h_{fin}/L_g is changed from 0.25 to 1.3. A taller FinFET structure induces an improvement in overall capacitance compared to gate electrode height along the channel sidewalls [21].

The cutoff frequency (f_T) dependence on transconductance (direct proportionality), as well as total capacitance (inverse proportionality), is shown in the form of equation given below (equation 3). The f_T vs gate voltage curve at $V_{ds}=0.5$ V is shown in Fig. 6. The point where the minimal gate drain/source capacitance [20] meets the maximum of transconductance is where f_T peaks. In contrast to the other structures investigated in our study representing better gate tunability and hence better transconductance and fewer parasitic gate capacitances.

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (3)$$

The value of f_{max} can be approximately conveyed in equation 4 as follows:

$$f_{max} = \frac{f_T}{\sqrt{4G_{ds} + 8\pi R_g C_{gd}}} \quad (4)$$

Though, the maximum oscillation frequency (f_{max}) degrades with minitarization of L_g which can be related to substantial degradation in output conductance.

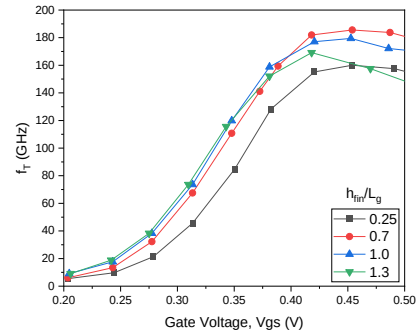


Figure 6. Proposed structure Cutoff frequency (f_T) as a function of gate voltage (V_{gs}) for $V_{ds}=0.05$ V

B. Impact of W_{fin}

The transverse electric field influence on the structure's source region can be reduced by using smaller W_{fin} values. Minor changes in device parameters such as W_{fin} and h_{fin} might cause significant differences in device performance. The influence of W_{fin}/L_g (0.25 to 1.0) and h_{fin}/L_g (0.25 to 1.3) changes on device performance metrics is investigated in this article, with the acquired $g_m - I_{ds}$ curves at $V_{ds} = 0.05$ V and 0.50 V displayed in Figure 7. Both the parameters g_m and I_{ds} are found to rise as

W_{fin}/L_g value increase. The W_{fin}/L_g value range chosen is the most effective in reducing SCEs. The detail about the series resistance [17] is also included in the graph.

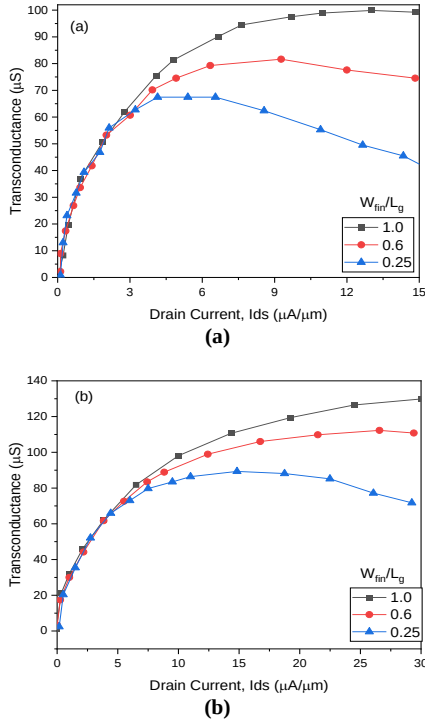


Figure 7. Proposed structure Transconductance (g_m) vs drain current (I_d) at variable drain voltage a) 0.05 V and b) 0.50 V for $L_g=22$ nm, $h_{fin}=22$ nm, $t_{ox}=0.9$ nm, $t_{box}=40$ nm, $t_{sub}=75$ nm, and gate to source voltage 0 V-to-0.5 V

Following that, the $g_{ds} - V_{ds}$ curves for various W_{fin}/L_g values are presented in Figure 8. The parameter g_d is proportional to W_{fin} , hence lower g_d values correspond to smaller W_{fin} values of the proposed structure. The device exhibits more variation in g_d values at higher V_{gs} values. It causes the device to heat up and produce more SCEs. As a result, the device V_{gs} values must be reduced to lessen the heating and SCEs influence, which limits the device width. Since C_{gg} does not affect DC performance. It has a direct effect on AC performance, much like the circuit's delay and switching time. [13].

Figure 9 shows the variance in the device's intrinsic gain A_v vs. V_{gs} for various values of W_{fin}/L_g (0.25 to 1.0) and $V_{ds}=50$ mV and 0.5 V. A bigger gain can be seen for devices that have a smaller width. Figure 10 shows the fluctuation in the

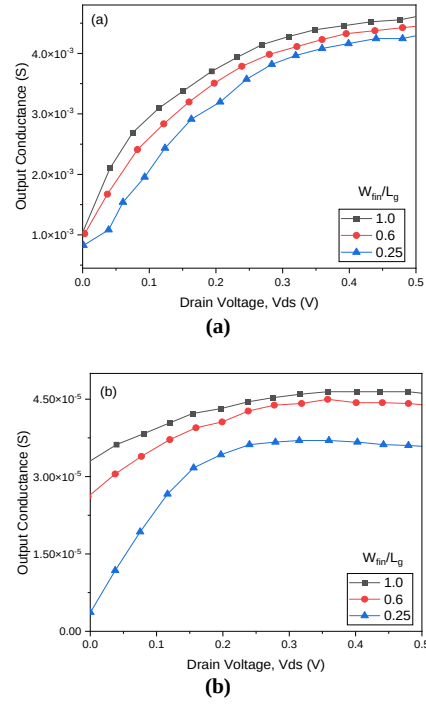


Figure 8. Proposed structure drain conductance (g_d) vs variable drain voltage a) 0.05 V and b) 0.50 V for $L_g=22$ nm, $h_{fin}=22$ nm, $t_{sub}=75$ nm, $t_{ox}=0.9$ nm, $t_{box}=40$ nm, and drain to source voltage 0V-to-0.7 V

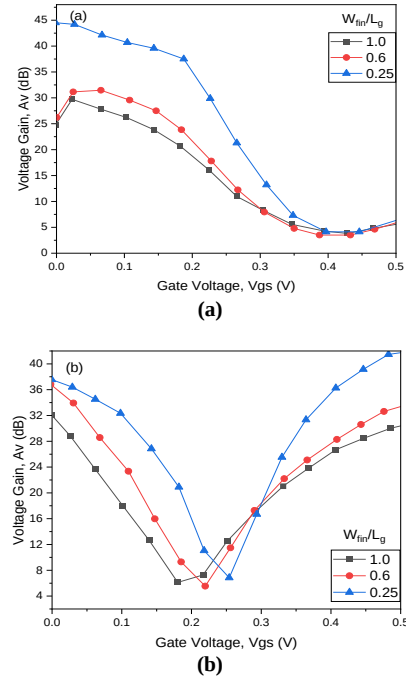


Figure 9. Proposed structure intrinsic gain A_v -gate voltage V_{gs} at a) $V_{ds} = 0.05$ V b) $V_{ds}= 0.50$ V for $L_g=22$ nm, $h_{fin}=22$ nm, $t_{ox}=0.9$ nm, $t_{box}=40$ nm, $t_{sub}=75$ nm, with $V_{gs} :0$ V-to-0.5 V

$C_{gg} - V_{gs}$ at different widths of devices with $V_{ds} = 0.05\text{ V}$ and 0.50 V . While altering W_{fin}/L_g from 0.25 to 1.0, the C_{gg} values are found to be lowered by 29 percent. The *fin* structures minimize the device's SCE and, as a result, the gate capacitance, which improves circuit latency [22], [23].

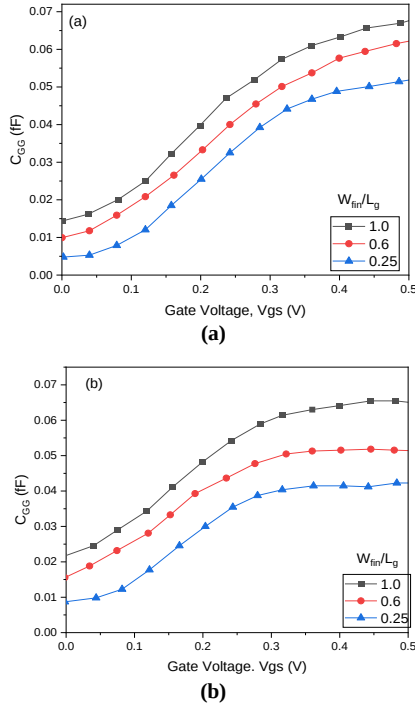


Figure 10. Proposed structure gate capacitance C_{gg} vs. gate voltage V_{gs} at a) $V_{ds} = 0.05\text{ V}$ and b) $V_{ds} = 0.50\text{ V}$ for $L_g = 22\text{ nm}$, $L_{un} = 5\text{ nm}$, $h_{fin} = 22\text{ nm}$, $t_{ox} = 0.9\text{ nm}$, $t_{box} = 40\text{ nm}$, $t_{sub} = 75\text{ nm}$, with $V_{gs} : 0\text{ V}$ to 0.5 V

Conclusion

The current paper simulated the SOI-FinFET device and investigated the effects of changing h_{fin} , W_{fin} , and the W_{fin}/h_{fin} ratio on device performance. The device has demonstrated optimum performance for (i) $h_{fin}/L_g = 0.7$ value by maximizing structure voltage gain and operable frequency; (ii) $W_{fin}/L_g = 0.6$ value improves structure transconductance, voltage gain, and output conductance, allowing the device to run without any short channel impacts. The simulation has identified that device length variations that can provide varied performances, such as larger devices favoring higher current

drivability and smaller devices being recommended for reducing SCEs and providing more device immunization.

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