

A NOVEL CROSS-CONNECTED T-TYPE ASYMMETRICAL MLI WITH REDUCED COMPONENTS FOR PV APPLICATIONS

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Abstract

We provide a new seventeen-level cross-connected T-type (CT-type) inverter with a lower device count (RDC) in this study. Just eight power switches, four self-balancing capacitors, and two DC sources are needed for the suggested design. It reduces the voltage stress on the switches by avoiding the need for an H-bridge to generate the negative half cycle, in contrast to traditional multilevel inverters. The distinctive feature of this topology is its asymmetrical cross-connected structure, enabling seventeen voltage levels with far fewer components while maintaining natural capacitor voltage balancing. By cascading capacitors and DC sources with the switches, the inverter achieves the desired output levels efficiently. Thanks to its strong self-balancing and high-voltage handling capability, the design is particularly well-suited for renewable energy integration into the grid. The gate driver signals are generated using level-shifted pulse width modulation. A comparative study demonstrates the advantages of the proposed topology over existing designs in terms of component count, driver requirements, and total standing voltage. Its practicality is confirmed through both simulation studies and a laboratory prototype.

Keywords: CT-type; Multilevel Inverter; Pulse Width Modulation; Reduced Device Count; Total Harmonic Distortion; Total standing voltage

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List of Abbreviations

MLI	Multilevel Inverter
FC	Flying Capacitor
CHB	Cascaded H-Bridge
NPC	Neutral Point Clamped
CT-type	Cross-Connected T-Type
RDC	Reduced Device Count
DC	Direct Current
THD	Total Harmonic Distortion
TSV	Total Standing Voltage
LS PWM	Level Shifted Pulse Width Modulation
PWM	Pulse Width Modulation
POD	Phase Opposition Disposition
RL Load	Resistive Inductive Load
IGBT	Insulated Gate Bipolar Transistor
CF	Cost Factor

Introduction

In today's high- and medium-voltage applications, multilevel inverters (MLIs) are essential. Due in large part to their capacity to provide high-quality, high-voltage outputs, they are widely used in electric vehicles, wind energy systems, active power filters, grid-connected photovoltaic (PV) installations, and induction motor drives (Gupta & Jain, 2014b; Kumar *et al.*, 2020; Rathore *et al.*, 2021; Rathore & Yadav, 2022a, 2022b). MLIs may provide a broad range of output voltage levels by combining many DC sources, semiconductor switches, capacitors, and diodes. Technically speaking, they have a number of benefits, including as high efficiency, modularity, lower total harmonic distortion (THD), and the capacity to provide higher voltage levels.

Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC), and Flying Capacitor (FC) are the three primary forms of MLIs. Because it reduces the drawbacks of NPC and FC designs—namely, high switching losses, DC voltage imbalance, and expensive capacitor requirements—the CHB topology has drawn more attention from researchers. In order to lay the groundwork for the suggested architecture, this study provides a brief review of both traditional and newly designed MLI topologies, as mentioned in (Kumar *et al.*, 2021a, 2021b).

Because of their greater dependability and adaptability, cascaded H-Bridge (CHB) inverters that use multiple DC sources are typically more appealing than single-DC multilevel inverters (MLIs). Within this category, asymmetric CHB configurations are particularly appealing, as they

simplify control compared to symmetric designs and can achieve higher voltage levels with fewer devices (Gupta *et al.*, 2016; Anand & Singh, 2020). However, the need for numerous independent DC sources is a significant drawback of CHB inverters.

Traditionally, MLIs faced challenges such as excessive DC source requirements and high semiconductor switch counts. In recent years, extensive research has focused on optimizing MLI structures to overcome these drawbacks. Several innovative configurations have been proposed, including switched-capacitor, switched-diode, and switched-DC designs (Gupta & Jain, 2014a; Mahato *et al.*, 2019; Siddique *et al.*, 2020b). For instance, the asymmetric MLI introduced in (Alishah *et al.*, 2017) reduces component count compared to conventional circuits. Cost-effective switched-DC topologies with improved performance have also been reported in (Babaei *et al.*, 2014a; Alishah *et al.*, 2015), offering both positive and negative voltage polarities even with fewer devices. Several fundamental units can be cascaded in series to produce higher voltage levels.

Optimized structures incorporating H-bridges, as presented in (Gautam *et al.*, 2016; Siddique *et al.*, 2020a), demonstrate the generation of 15 voltage levels using 7 DC sources and 16 switches in a basic unit. By modifying DC source arrangements, these designs reduce switching stress while maintaining flexibility. Symmetrical and asymmetrical topologies employing various pulse width modulation (PWM) techniques have been validated in (Saeedian *et al.*, 2017; Salem *et al.*, 2021; Vemuganti *et al.*, 2021). Further, switched-DC-based designs capable of replacing traditional MLIs have been investigated in (Babaei *et al.*, 2015; Samadaei *et al.*, 2019; Routray *et al.*, 2020). In (Pulikanti & Agelidis, 2011), a simplified two-switch setup coupled by a DC link was suggested, and an H-bridge was included to produce negative voltage levels. This design was later enhanced in (Omer *et al.*, 2020) by adding two capacitors, enabling additional voltage levels per module.

Multiple voltage levels can be produced by combining conventional multilevel inverters (MLIs) in hybrid configurations. A few hybrid topologies described in (Meraj *et al.*, 2017) fall under the category of symmetrical MLIs. These symmetric arrangements can reach higher voltage levels with a lower device count (RDC) by using uneven DC input voltages. In (Babaei *et al.*, 2014b), an unusual asymmetrical topology was presented, in which power switches are set up to provide larger voltage levels while reducing the strain on semiconductor components. Similar to this, unequal DC supplies are incorporated into a modified H-bridge

architecture presented in (Hosseinzadeh *et al.*, 2021), which causes different bridges within symmetrical MLIs to operate at different voltage levels.

The basic design goal of MLIs may be jeopardized in these situations since the switches connected to the high-voltage bridge must endure increased stress, especially when low-rating switches are employed in high-power applications. Asymmetrical MLIs that depend on voltage balancing techniques also exhibit this disadvantage. However, self-balancing bridges with equal DC-link voltages, mainly constructed in symmetrical designs, are used in the asymmetrical MLIs described in (Babaei *et al.*, 2014b; Meraj *et al.*, 2017; Hosseinzadeh *et al.*, 2021). Consequently, inverter control is made simpler because no extra balancing circuits are needed.

The goal of the suggested multilevel inverter (MLI) is to increase output voltage levels while guaranteeing an effective configuration of semiconductor switches. Its cost-effective design reduces the quantity of power devices needed. Asymmetrical cross-connected T-type (CT-type) MLI configurations are shown in this study.

Nine different voltage levels (one zero, four negatives, and four positive) can be produced in the symmetrical setup by using two DC voltage sources and four capacitors with identical ratings. The DC voltage sources of the CT-type module have a 1:3 ratio for the asymmetrical design. The inverter may generate seventeen voltage levels with this configuration: eight negative, eight positive, and one zero.

The fact that the CT-type modules naturally produce the negative half cycle without the need for an extra cascaded H-bridge stage is a major benefit of the suggested design. The system is small and economical because it only requires eight switches, four capacitors, and two DC sources, to achieve this performance.

The structure of this paper is organized to guide the reader progressively from design to validation. Section 2 introduces the circuit configuration and operating principle of the proposed CT-type MLI, including its asymmetric arrangement, modes of operation, and module extension for generating output voltage levels. Section 3 explains the modulation and control strategies, followed by simulation results that demonstrate the inverter's performance. Section 4 presents the experimental test rig and laboratory prototype outcomes, while Section 5 provides a detailed analysis of power loss and efficiency.

Section 6 offers a comprehensive comparative study of recent MLI topologies against the proposed CT-type configuration. Finally, Section 7 concludes the paper with key findings and future directions.

Generalised Topology of the Proposed MLI

Circuit configuration and its working

The schematic of a simple CT-type multilevel inverter is shown in Figure 1(a). One DC supply, two unidirectional switches, two capacitors, and one bidirectional switch are used to construct the setup. The bidirectional switch connected to the DC supply plays a crucial role in ensuring safe operation, as it blocks current flow in both directions and thereby prevents short-circuit conditions. In addition, the use of DC-link capacitors in this design naturally maintains voltage balance without requiring any external circuitry. The module may generate a three-level output voltage waveform with this configuration. Figure 1(b) highlights different possible placements of the bidirectional switches, demonstrating the flexibility of the proposed inverter structure.

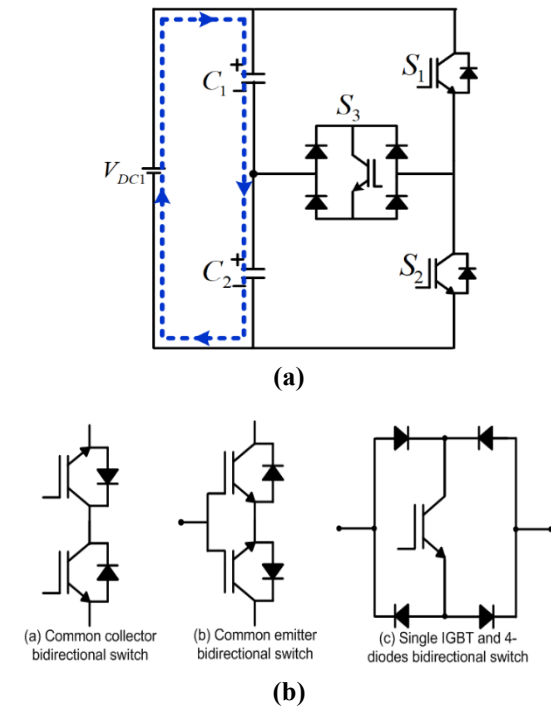


Figure 1. (a) Basic cell of single-phase CT-type multilevel inverter, (b) Various arrangements for bidirectional switches

Figure 2 depicts the generalized structure of the proposed asymmetric single-phase CT-Type MLI module. Two power switches connect the two fundamental modules, L and R. Unidirectional switches S1 and S2 connect the L and R modules, and vice versa. The load (L and R) is connected to both modules. Despite having fewer power devices, this configuration may generate numerous voltage levels. Low switching frequency and total harmonic distortion (THD) are predicted to be greatly reduced at higher voltage levels.

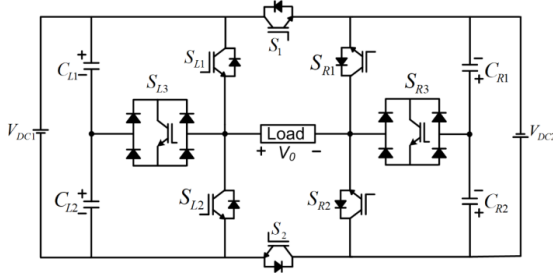


Figure 2. Generalized single-phase CT-Type MLI module

Analytical Analysis of Capacitors Values

The capacitor starts to charge and discharge when connected in series with the load and in parallel across the voltage source (Kumar *et al.*, 2021b). The charging and discharging of the capacitor have a significant impact on the output voltage levels in the proposed CT-type MLI. Determining the appropriate capacitor value is so essential. The capacitance value is determined by the operating frequency and the load current. According to (Rathore *et al.*, 2021), the discharging phase is when the capacitor experiences the most voltage ripple. Consequently, the capacitance value is determined using the capacitor's worst-case discharge duration. The voltage ripple must be within a specific range in order to be considered acceptable. Maintaining a low ripple voltage reduces losses and boosts the efficiency of the proposed topology. As seen in Figure 2, both capacitors are connected in series with the DC input voltage source. As a result, both receive the same current when charging, which causes the same charge to accumulate on them. Therefore,

$$I_{C1} = I_{C2} \Rightarrow Q_{C1} = Q_{C2} \Rightarrow C_1 V_{C1} = C_2 V_{C2} \quad (1)$$

Uniform capacitance selection ensures the applicability of eq. (1)

$$\begin{cases} C_1 V_{C1} = C_2 V_{C2} \\ V_{C1} = V_{C2} \end{cases} \Rightarrow C_1 = C_2 \quad (2)$$

Therefore, eq. (2) shows that both capacitors have the same value $C_1 = C_2$. The maximum charge stored in each capacitor can be written as:

$$\Delta Q_C = I_L \int_{t_s}^{t_f} \sin(2\pi f_0 t) dt \quad (3)$$

Here $[t_s, t_f]$ represents the time interval corresponding to the most critical operating condition for each capacitor. The terms I_L and f_0 represent the output fundamental frequency and the load current amplitude, respectively. It is important to highlight that both capacitors have equal capacitance values $C_1 = C_2$. Once the load is connected, the equivalent capacitance (C_{eq}) can be written as:

$$C_{eq} \geq \frac{\Delta Q_C}{K V_{eq}} \quad (4)$$

For a purely resistive load, the output current can be expressed as:

$$I_L(t) = \begin{cases} \frac{V_{dc}}{R_L} & \text{for } t_1 \leq t \leq t_2 \\ \frac{2V_{dc}}{R_L} & \text{for } t_2 \leq t \leq t_3 \\ \frac{3V_{dc}}{R_L} & \text{for } t_3 \leq t \leq \frac{T}{4} \end{cases} \quad (5)$$

In the case of a resistive-inductive load, the output current can be expressed as:

$$I_L(t) = I_{\max} \sin(\omega t - \alpha) \quad (6)$$

Eq. (7) provides the suitable range of capacitor values for both RL and purely resistive loads. These ranges are derived by considering the most critical operating conditions, so that each capacitor can store sufficient charge and maintain voltage balance during inverter operation.

$$C_1 = C_2 \geq \frac{2 \int_{t_3}^{T/4} I_L(t) dt}{K V_{eq}} \quad (7)$$

The circuit parameters are selected for the suggested CT-type inverter topology as $R=20\Omega$ and

40 Ω , $L=20\text{mH}$ and 40mH , coupling coefficient $k=0.05$, and reference frequency $f_{\text{ref}} = 50 \text{ Hz}$. The equivalent capacitance is obtained when two identical capacitors are connected in series, denoted as $C_1 = C_2 \geq 1780 \mu\text{F}$. To ensure proper operation with the given load and to maintain a capacitor voltage ripple within 5%, at least two identical capacitors must be selected. Consequently, the closest commercially available capacitance value is used for both modeling and experimental validation

in Sections 3 and 4.

Circuit Asymmetric CT-Type Topology

Figure 3 shows the proposed 17-level asymmetrical CT-type multilevel inverter, where the active current paths are highlighted in red. The different switching states are listed in Table 1. In this configuration, the R-module operates with DC-link voltages of ($V_{C1R} = V_{C2R} = 3E$), while the L-module operates with DC-link voltages of E ($V_{C1L} = V_{C2L} = E$).

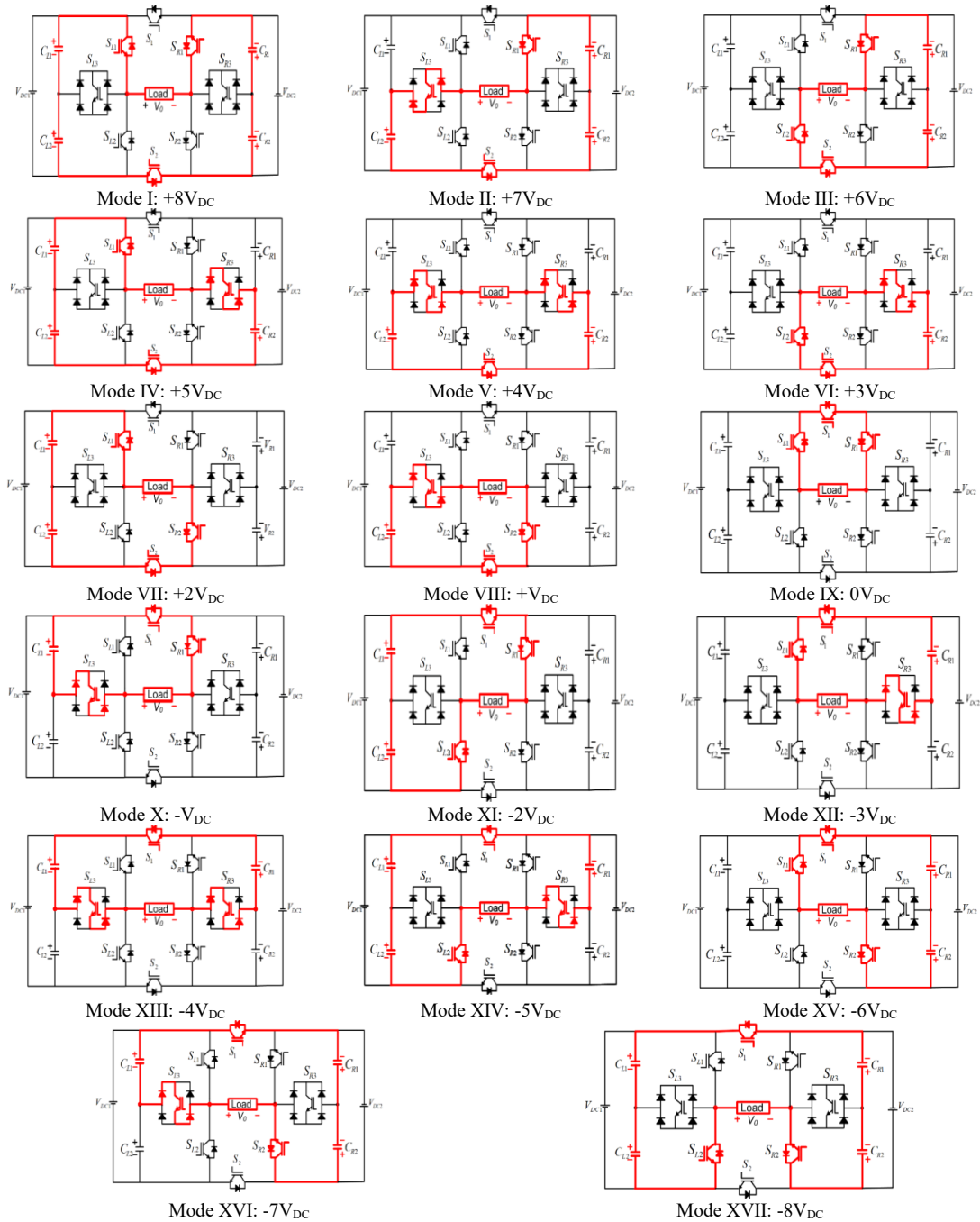


Figure 3. Different Switching States

Table 1. Different Modes of 17-level Asymmetric Topology

MODE	Capacitor Behavior	Output Voltage	Switch Condition
I	All capacitors discharging	(+8E)	All upper switches ON
II	C _{R1} , C _{R2} discharging	(+7E)	One R-module switch OFF
III	C _{R1} , C _{R2} discharging	(+6E)	Alternate switches ON
IV	C _{L1} discharging	(+5E)	L-module partially ON
V	C _{L2} , C _{R2} discharging	(+4E)	Balanced conduction path
VI	C _{L2} discharging	(+3E)	Reduced ON switches
VII	C _{L1} discharging	(+2E)	Further reduction
VIII	C _{L1} / C _{L2} slight discharge	(+E)	Minimal conduction path
IX	Neutral (no net charge)	(0)	Symmetrical ON/OFF
X	Capacitors charging	(-E)	Mirror of State VIII
XI	C _{L1} charging	(-2E)	Mirror of State VII
XII	C _{L2} charging	(-3E)	Mirror of State VI
XIII	C _{L2} , C _{R2} charging	(-4E)	Mirror of State V
XIV	C _{R1} charging	(-5E)	Mirror of State IV
XV	C _{R1} , C _{R2} charging	(-6E)	Mirror of State III
XVI	C _{R1} , C _{R2} charging	(-7E)	Mirror of State II
XVII	All capacitors charging	(-8E)	All lower switches ON

Voltage Stress Calculation

The maximum voltage blocking capacity of the switches in the OFF state is known as the TSV under asymmetric operation. These separate blocking voltages are added up to determine the overall TSV of the suggested CT-type MLI. The computation can be written like this:

Switches S₁ and S₂ must both be able to tolerate a blocking voltage of 2E in this setup. Because Switch S₃ is connected across the capacitors of the 3E module, it is subject to a greater stress of 6E. These blocking voltages are then added together to determine the TSV of the inverter.

$$V_{S1} = E + E = 2E, V_{S2} = E + E = 2E, V_{S3} = 3E + 3E = 6E \quad (8)$$

Switch S₄ also blocks 6E (similar to S₃). Switch S₅ experiences the highest stress (8E) because it spans both modules (1E and 3E sources plus their capacitors).

$$V_{S4} = 3E + 3E = 6E, V_{S5} = E + E + 3E + 3E = 8E, \quad (9)$$

Summing all eight switches gives the total standing voltage of 36E. This means the inverter requires switches with sufficient reverse blocking capability to withstand this cumulative stress.

$$TSV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} + V_{S7} + V_{S8} = 36E \quad (10)$$

Simulation Study

Modulation and Control Method of MLI

Several modulation techniques are available for controlling multilevel inverters. Multi-carrier PWM and space-vector PWM are high-frequency techniques; nearest-level control, selective-harmonic elimination, active-harmonic elimination, and Low-frequency techniques include nearest level control (NLC), selective harmonic elimination (SHE), and active harmonic elimination (AHE). Although any of these methods can be applied to the suggested CT-type inverter, level-shift PWM (LS-PWM) is used in this work. LS-PWM generates gate pulses for switches at various voltage levels by comparing triangular carrier signals to a sinusoidal reference signal. The modulation index (MI) is computed using equation (11), and the reference waveform's peak is denoted by V_{ref, peak}.

$$MI = \frac{V_{ref, peak}}{8V_{car}} \quad (11)$$

In the proposed inverter, gate pulses are generated using the phase-opposition disposition (POD) method. Figure 4(a) shows the schematic of the control approach, and Figure 4(b) depicts the LS-PWM waveform in the time domain. Because multiple switching states can produce the same voltage level, one particular state is chosen to reduce unnecessary transitions between higher and lower

voltage levels in the IGBTs. The PWM signals for switches S1 to S8 are assigned based on the placement of the high-frequency carrier signals relative to the sinusoidal reference.

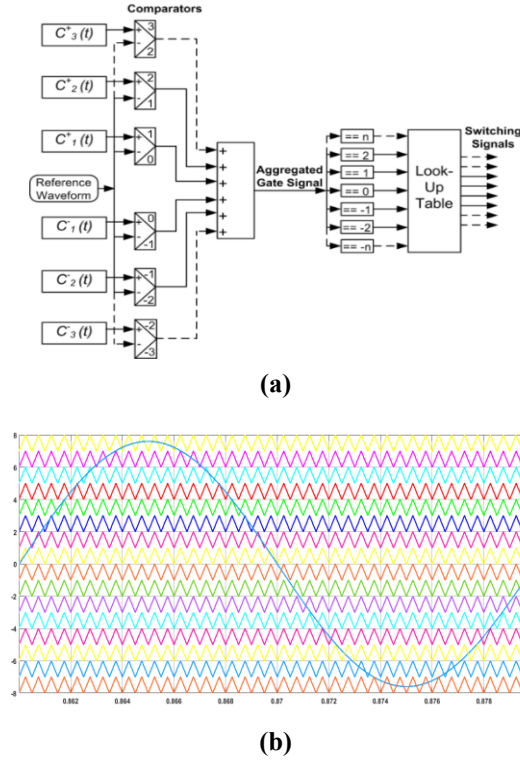


Figure 4. (a) Block diagram of control method (b) Corresponding waveform.

Simulation Results

LS-PWM modulation was used in MATLAB/Simulink to implement the suggested CT-type inverter. Table 2 contains a list of simulation parameters. Two DC sources, $V_{DC1} = 24$ V and $V_{DC2} = 72$ V, were utilized for asymmetrical arrangement in order to get the required output. The 17-level output voltage waveform, where the peak voltage reaches $V_{BB} = 96$ V, is displayed in Figure 5(a). Figure 5(b) displays the equivalent load current waveform. The capacitor voltages in the asymmetrical design are depicted in Figures 6(a) and 6(b), with C_{L1} and C_{L2} in Figure 6(a) and C_{R1} and C_{R2} in Figure 6(b).

The 17-level output voltage and related load current are displayed in Figures 5(a) and 5(b). These findings verify that the suggested CT-type inverter can produce high-quality, smooth waveforms with less harmonic distortion. The capacitors' ability to self-balance is further demonstrated in Figures 6(a) and 6(b), where their voltages stay constant within the permitted ripple range. Overall, the findings verify that the proposed topology delivers

dependable multilevel operation while requiring fewer components.

Table 2. Parameters of Simulation

Parameter	Value
Rated DC voltage	$V_{DC1} = 24$ V & $V_{DC2} = 72$ V
Capacitors	$C_1 = C_2 = 2200 \mu F$
Modulation index	$m_a = 0.85$
Load value	L= 20 mH, R=20 Ω
Modulating wave frequency	$f_m = 50$ Hz
Switching frequency	$f_s = 3150$ Hz

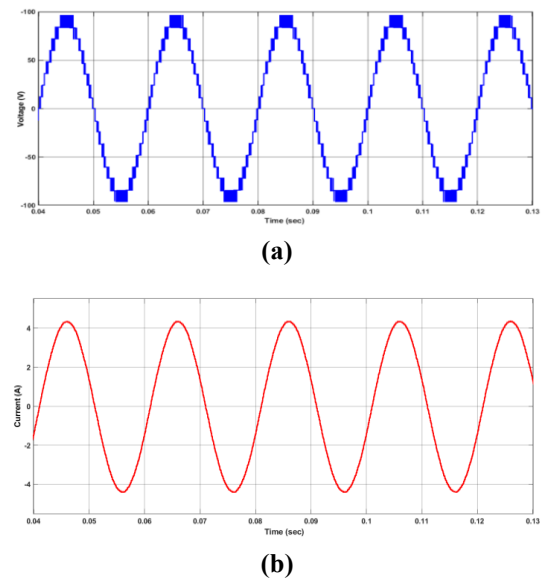


Figure 5. (a) Output voltage (b) Load Current

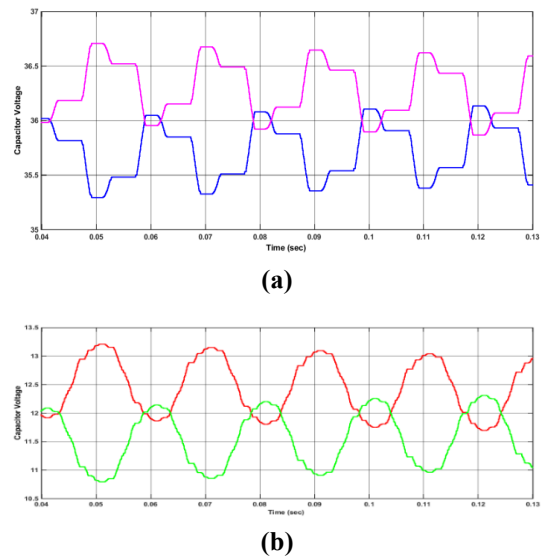


Figure 6. Voltage across capacitors (a) C_{L1} and C_{L2} (b) C_{R1} and C_{R2}

Experimental Setup Results

A laboratory prototype was constructed using power switch modules, gate drivers, and separated power sources in order to experimentally validate the suggested CT-type inverter. Figure 7 depicts the overall configuration, while Table 3 summarizes the component values. To ensure that the practical results match the simulation, the simulated gate pulses and control signals were transferred directly to the hardware using a dSPACE-1104 controller.

Table 3. Parameters of Experimental Setup

Parameter	Value
Single-phase power analyzer (Fluke)	-
Load (RL Load)	R= 40Ω, L= 40 mH R= 20Ω, L= 20 mH
Controller board (dSPACE-1104)	-
Digital storage oscilloscope (DL-750E)	6-channel
IGBT switch (GW30NC120HD)	1200V, 30A
Switching frequency	3150 Hz
Output voltage frequency	50Hz
Driver circuit (TLP250(F))	10-35 V
DC Source (lead acid battery)	28 Ah
Capacitor (LGU2A222MELA)	2200 μF

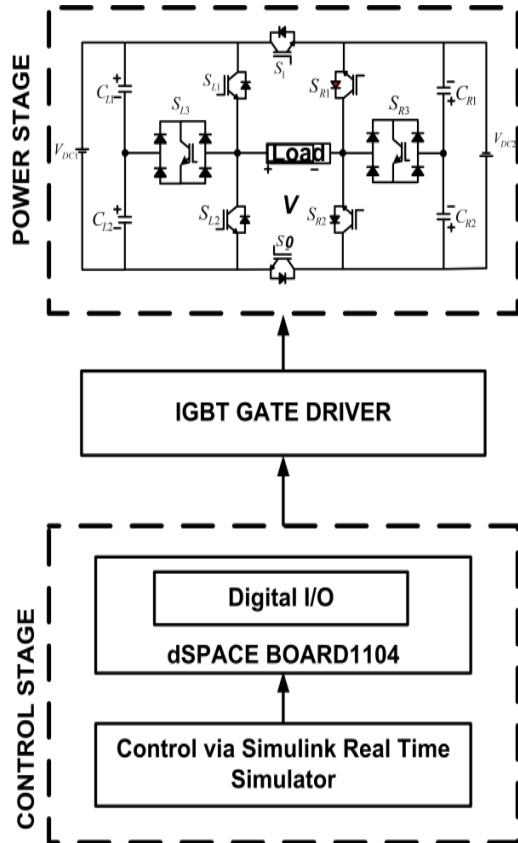


Figure 7. Block Diagram of the experimental setup

In the asymmetric prototype, the DC-link voltages are configured as $V_{C1L} = V_{C2L} = 24V$ and $V_{C1R} = V_{C2R} = 72V$, resulting in a total DC-link voltage of 96 V. The inverter output is connected to a single-phase RL load with $R = 40\Omega$ & 20Ω and $L = 40mH$ & $20mH$.

Figures 8 and 9 present the experimental waveforms of capacitor voltage, output voltage, and load current under both steady and dynamic load conditions. Harmonic analysis results are shown in Figures 9(a) and 9(b), where the voltage THD is measured at 7.2% and the current THD at 1.3%. These values confirm the inverter's ability to deliver high-quality output with low distortion.

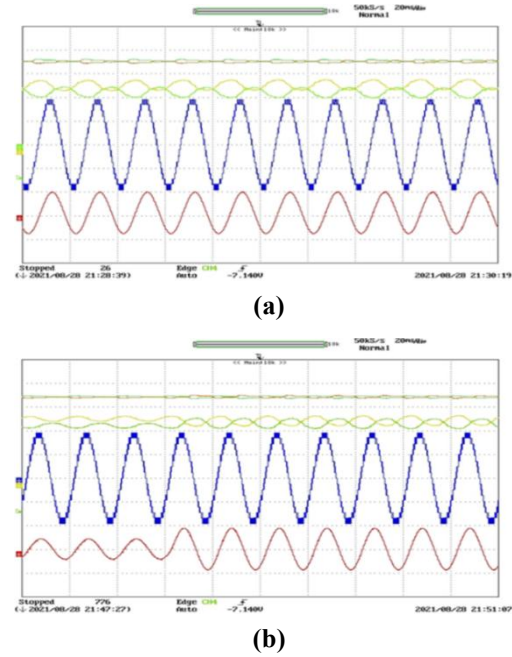


Figure 8. Experimental results (a) capacitors voltage (C_{L1} and C_{L2}), load current, and output voltage with ($R= 20\Omega$, $L= 20$ mH) (b) capacitors voltage of (C_{R1} and C_{R2}), load current, and output voltage with ($R= 40\Omega$, $L= 40$ mH).

Loss Calculation

Switching losses and conduction losses are the two main forms of losses connected to the power switches in the suggested CT-type topology. When switches are in the ON state, current flows through them, causing conduction losses (PC). The equivalent load current in each MLI switch is conducted by both the IGBT and its anti-parallel diode. Consequently, the conduction losses of the diode (PC, D) and the IGBT (PC, IGBT) are added to determine the total conduction loss. These can be approximated as follows:

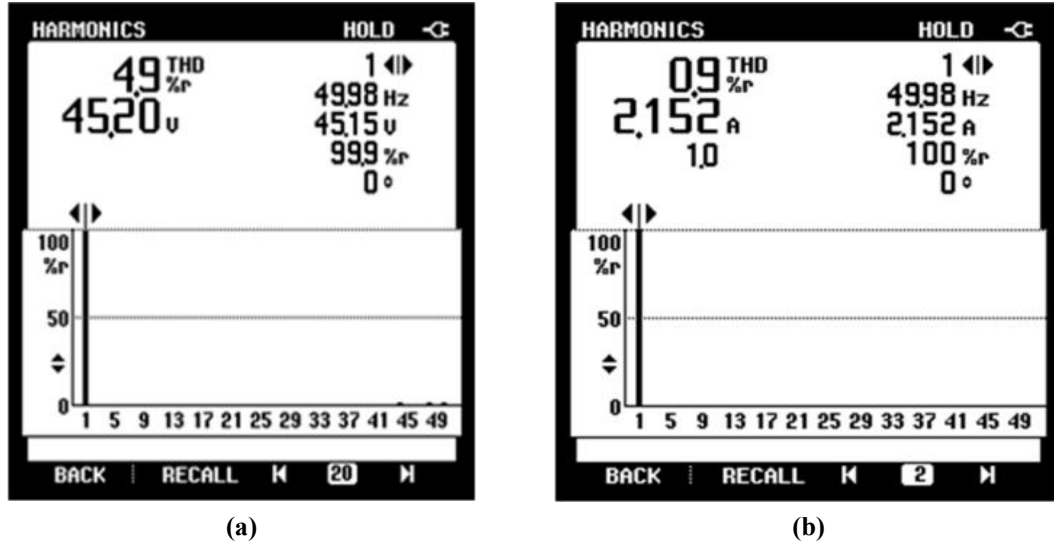


Figure 9. Experimental results with load ($R= 20\Omega$, $L= 20 \text{ mH}$) showing: (a) Output voltage THD (b) Output current THD

(a) Switching losses:

Power switches experience switching losses whenever turned on and off (Mahato *et al.*, 2019). These losses are expressed:

Where, P_{s_on} , P_{s_off} are the terms used to describe the power losses associated with the switch on and off, respectively.

$$P_{s_on} = \frac{f_0}{6} V I_{s_on} t_{on} \quad (12)$$

$$P_{s_off} = \frac{f_0}{6} V I_{s_off} t_{off} \quad (13)$$

Finally, the total switching losses:

$$P_s = \sum (P_{s_on} + P_{s_off}) \quad (14)$$

Where, f_0 : fundamental frequency.

t_{on} , t_{off} : turn-on/off time.

V : blocking state voltage.

I_{s_on} , I_{s_off} : currents that flow through the switches after and before they are turned on and off, as appropriate.

(b) Conduction losses (P_c):

The internal resistance of the transistors generates this sort of loss. (R_s) and diodes (R_d) (Mahato *et al.*, 2019). The losses resulting from switches and diodes can be quantified in numerical terms as follows:

$$P_{s_c} = V_{s_on} I_{s_avg} + R_{s_on} I_{s_rms}^2 \quad (15)$$

$$P_{d_c} = V_{d_on} I_{d_avg} + R_{d_on} I_{d_rms}^2 \quad (16)$$

Overall conduction losses

$$(P_c) = P_{s_c} + P_{d_c} \quad (17)$$

An on-state resistance value for the transistor or diode is represented by R_{s_on} , and R_{d_on} .

V_{s_on} , V_{d_on} : on-state voltage drops across the transistor and diode, respectively.

The rms and average currents through switches are denoted by I_{s_rms} and I_{s_avg} .

Average and rms diode current, respectively, are I_{d_avg} and I_{d_rms} .

(c) Ripple losses (P_r):

Equation (18) describes the ripple loss during capacitor charging/ discharging (Mahato *et al.*, 2019).

$$P_r = \frac{f_r}{2} C (\Delta V_c^2) \quad (18)$$

The overall effectiveness can be represented as follows:

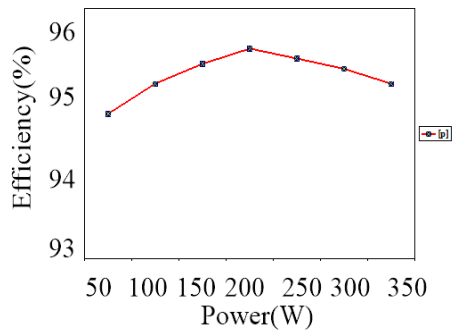
$$\% \eta = \frac{P_{out}}{(P_{out} + total \ losses)} \times 100 \quad (19)$$

The efficiency study for output power ranging from 50W to 350W is presented in Figure 10.

The graph illustrates the relationship between efficiency and output power. According to Figure 10, the proposed topology achieves a maximum efficiency of 95.85% at an output power 200W. At an output power of 350W, the efficiency tested was 94.7%.

Table 4. Comparison of topologies (MLIs) to generate 17-level output based on the component requirement

Topologies	Diode Clamp MLI	Cascaded H- bridge MLI	Flying capacitor MLI	Babaei <i>et al.</i> (2014b)	Hosseinzadeh <i>et al.</i> (2021)	Proposed CT-type MLI	
Driver circuit	32	32	32	12	10	8	
TSV	32	32	32	40	36	36	
Capacitors and DC supplies	16	8	16	4	4	6	
Power switches	32	32	32	12	10	8	
Diodes	48	32	32	12	14	8	
Total components	96	72	80	28	28	22	
CF/ Level	$\alpha=0.5$	6.57	5.18	5.63	2.82	2.7	2.47
	$\alpha=1$	7.51	6.1	6.59	4	3.76	3.52
	$\alpha=1.5$	8.48	7.04	7.51	5.17	4.82	4.58

**Figure 10. Efficiency Curve**

Comparison Assessments

The suggested CT-type inverter is contrasted in this section with other popular multilevel inverter designs, such as those described in (Hosseinzadeh *et al.*, 2021) flying capacitor, diode-clamped, and cascaded H-bridge. The findings demonstrate that compared to traditional designs, the CT-type inverter may provide higher voltage levels with fewer components. For example, producing a 17-level output requires only 22 components in the CT-type inverter, which is much lower than in other topologies and those described in (Routray *et al.*, 2020). One trade-off is that the CT-type inverter has a higher TSV, meaning that switches with stronger reverse blocking capability must be used. To assess cost-effectiveness, the cost factor (CF) is calculated using eq. (20).

$$CF = \frac{[N_{dc} + N_s + N_{dio} + N_{cap} + \alpha(TSV)] * nV_{dc}}{N_{levels}} \quad (20)$$

“Ndio” represents the total number of diodes, “NS” represents the total number of switches, “Ncap” represents the number of capacitors,

“NDC” represents the number of DC supplies, “ α ” represents the weight coefficient, and “TSV” represents the total standing voltage. Show in Table 4.

Conclusion

This work introduces a single-phase CT-type multilevel inverter that uses fewer components while still delivering reliable performance. The design principles, control strategy, and voltage-handling capability have been discussed, and the capacitors are shown to balance themselves naturally. One of the main benefits is that the inverter can generate negative voltage levels without needing a modified H-bridge. The modular structure also allows the design to be scaled up to higher voltage levels, such as 17 and even 289 levels, while keeping the device count low. This makes the inverter especially suitable for renewable energy and high-power applications. Both simulations and experiments confirm its effectiveness under different load conditions. When compared with other recent inverter designs, the CT-type inverter stands out because it requires fewer switches, drivers, capacitors, and DC sources, making it simpler and more cost-effective. Overall, the proposed topology performs reliably and efficiently in a wide range of operating scenarios.

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Santosh Kumar Gupta: Supervision, Manuscript Review.

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Ethics Approval and Consent to Participate

This study is based entirely on computational simulations in MATLAB software. It does not involve human participants, animals, biological samples, or collection of personal data. Therefore, ethical approval from an institutional ethics committee was not required.

Declaration of Generative AI

The authors declare that no Generative AI tools were used in the preparation of this manuscript.

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