

DESIGN AND ANALYSIS OF ELECTRICAL CHARACTERISTICS OF INVERTED-T JUNCTIONLESS (JL) FET THROUGH GEOMETRIC AND PROCESS VARIATIONS FOR HIGH FREQUENCY APPLICATIONS

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Abstract

An inverted-T structure is implemented with the Junctionless (JL) topology at nanoscale dimensions. The Inverted-T Junctionless (ITJL) FET features a multi-fin architecture that utilizes the unused space within the fins and combines it with the junctionless topology, maintaining the same doping concentration from source to drain. In order to mitigate the short channel effects and overcome the fabrication challenges, an inverted-T FET has been designed. The crucial performance parameters of device are explored by varying the geometric dimensions and process parameters. The performance of ITJLFET is measured by varying different parameters namely temperature (T), doping concentration (N_d), work function (ϕ_m), and dielectric constant (K) at 30-nm technology node and effect of geometric variations are measured by altering the gate length (L_g) and oxide thickness (T_{ox}). Inverted-T junctionless field effect transistor (ITJLFET) is designed with different gate lengths in the range of 14 nm to 30 nm and shows the improvement in I_{ON} by 64% as compared to the conventional JLFET. The parametric analysis like transfer characteristics (I_d-V_{gs}), I_{on}/I_{off} ratio, subthreshold swing (SS), drain induced barrier lowering (DIBL) and gate capacitance (C_{gg}) are investigated for 250 K to 350 K. From the results, it is perceived that temperature has less effect on the Inverted-T junctionless transistor performance. The cut-off frequency for the designed device is calculated and observed to be in the range of 0.3 to 1.5 THz. Hence, device can be used for high-frequency applications at the submicron regime.

Keywords: Analog performance; Inverted-T junctionless transistor; process variation; short channel effects

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Introduction

Transistor continues to be a vital parameter for the silicon industry for the past few decades (Bhuyan, 2017). With the advancement in technology, the size of MOSFET is shrinking by Moore's Law which states that the number of transistors on a microelectronic chip increases exponentially (Moore, 1965). Shrinking of transistor for the planar MOS structure largely followed the "Dennard Predictions" for structural dimensions (Schuegraf *et al.*, 2013). The scaling of the MOSFET device invites significant challenges such as short channel effects and an increase of leakage current, as the gate control weakens over the channel. This ultimately hampers the technological development (Bagga *et al.*, 2017). These challenges motivated the researchers to find new pathways to achieve desired performance at scaled channel length. Several architectures have been proposed by the researchers such as Tri-Gate (TG), SOI (Silicon on Insulator), FinFET, Junctionless FET, etc (Vandana *et al.*, 2017; Sahay and Kumar, 2019b). The aforesaid architectures gathered attention because these structures were able to match up with the characteristics of traditional MOSFET I-V. The proposed architectures can restrain the Short Channel Effects (SCE) and offer an approximately ideal Subthreshold Slope (SS) with diminished off-state leakage current at sub-10 nm regime (Wong *et al.*, 1998).

The basic architecture of MOSFET encompasses two junctions i.e. source-channel junction and drain-channel junction (Sahay and Kumar, 2019a). At these junctions, there is a steep change in the doping profile and the fabrication of such a device at a lower technology node is a challenging task while maintaining its electrostatic properties (Bharath and Narendar, 2021; Kumar and Kumar, 2021a; Vakkalakula and Vadthiya, 2021). However, the main challenge faced by the silicon industry while performing the downsizing of the MOSFET is improving its electrical performance. In the submicron regime maintaining control over factors such as tunnelling of hot electrons, trapping of charge in interface states, subthreshold leakage current, and DIBL is an extremely challenging and costly affair (Choi *et al.*, 2011; Trevisoli *et al.*, 2011). The fabrication of Junction-based transistors at the decananometer technology length requires high-end lithographic techniques, thereby increasing their manufacturing cost. Along with this, a steep change in the doping profile enforces the challenge on doping techniques and enhances the thermal budget (Nelapati and K, 2020; Trevisoli *et al.*, 2011; Bashir *et al.*, 2022).

To address both performance and fabrication challenges, a "Device controlling electric current" utilizing a gated resistor was initially proposed by Lilienfeld and Colinge (2012) at Tyndall University followed by CEA-LETI group named the device as 'Junctionless Nanowire Transistor' in 2009 (Lilienfeld, 1925; Lilienfeld, 1928; Colinge *et al.*, 2010; Vandana *et al.*, 2017). They have delivered an experimental study to demonstrate no doping gradient across the junctionless nanowire transistor. These transistors assured enhanced performance at the submicron regime and exhibit improved device characteristics (Agnihotri and Tripathi, 2019; Colinge *et al.*, 2011). The major challenges faced are lower off-state leakage current, less mobility deterioration, and a nearly ideal value of subthreshold slope under bias conditions at scaled channel length. If these challenges are not suppressed with creative and innovative techniques, it jeopardizes the advantages of Moore's Law (Schuegraf *et al.*, 2013; Pal *et al.*, 2014).

Accordingly, a device was designed by Zhang *et al.* (2006) featuring a multi-fin architecture on a single substrate that amalgamates the advantages of 3D architectures with UTB (Ultra-thin Body). These architectures are commonly known as inverted-T (IT) FET which boosts the electric field in both horizontal and vertical channels. ITFET tends to provide high I_{ON} , efficient chip area utilization, and better electrostatic control compared to traditional FinFET by utilizing the unused area between the fins (Vandana *et al.*, 2018).

In order to overcome the fabrication issues at nanoscale regime due to density gradient at the source-channel and drain channel junctions, the designed device utilizes the junctionless topology. Additionally, it incorporates the inverted-T topology which makes use of the unwanted area among the fins to create an ultra-thin body device that effectively mitigates short channel effects. The inverted-T topology eradicates the limitation of FinFET by utilising the space between the fins. The present work combines the inverted-T topology and junctionless topology, resulting in the structure of the inverted-T junctionless FET (ITJLFET) device. In the present work, an inverted-T Junctionless FET (ITJLFET) device is designed and its performance has been measured. To enhance the electrical property of ITJLFET, a high- κ oxide is used to improve the electrostatic integrity and gate control over the channel. To measure the device performance, various process parameters are adjusted. The study assesses the device performance by analysing different parameters including drain

current (I_{on}), drain-induced barrier lowering (DIBL), leakage current (I_{OFF}), subthreshold slope (SS), oxide capacitance (C_{gg}), threshold voltage (V_{th}) and transconductance (g_m). In 2018, Vandana *et al.* (2018) measured the performance of IT junctionless transistors through device geometry variation. In this work, the performance measurement of IT junctionless transistor is investigated through the process and geometric variations.

Apart from the introduction, section II discusses the technology roadmap to advance computing technology. Section III specifies the details of the designed device and physical insight of the models used for the simulation. The device characteristics and result analysis has been done in section IV and the impact of process variations is presented in section V along with a comparison with literature. At last, the conclusion is drawn.

Technological RoadMap

Figure 1 demonstrates the technological developments that have occurred in the recent decades and offers alternatives for the essential components required in the designing of transistors. In the recent years, semiconductor device manufacturing has been fundamentally driven by logic technology for the past few years. It's important to note that the roadmap presented does not specifically attribute the development to any particular semiconductor device inventor.

While studying the manufacturing roadmap at the initial level, wafer scaling is observed, which involves transitioning from 300 mm to 450 mm wafers. This demand is enforced by the rapid increase in process complexity and manufacturing cost (ITRS, 2015).

Secondly, after modification of wafer manufacturing necessitates an alteration in the transistor manufacturing techniques. Transistor manufacturing has moved to single-wafer processing due to the requirement for novel materials and high precision in structural dimensions. SiGe is introduced to enhance the channel mobility and the gate is constructed using metal to scale the effective oxide thickness (EOT) of the gate dielectric. New FET architectures have been proposed, prompting the semiconductor industry to migrate from MOSFET to FinFET architecture. The FinFET architecture, a 3D design, offers superior electrostatic control. However, it is less effective with the technology nodes below 5 nm and it leading to the development of GAA, commonly known as nanowire transistor (Kuhn *et al.*, 2012; Shankar *et al.*, 2014).

Going forward to interconnects, copper dual damascene (Andricacos *et al.*, 1998) worked perfectly for 300mm wafers but it introduced RC-delay at the 22nm and 14nm technology nodes, which has become a significant concern for circuit engineers (Bohr, 1995; Kaushik *et al.*, 2007). An alternative of copper dual damascene is under investigation and can be a viable solution.

Earlier, embedded SRAM attained a lot of attention because of its compatibility with digital CMOS. For various high-end applications, DRAM is preferred due to its high density and power performance (Matick and Schuster, 2005). As technology length is reduced for optimizing the power in the circuit, SRAM exhibits marginal performance. To overcome the imperfections in the SRAM circuit, the invented Transfer-Torque MRAM has gained the interest of embedded design engineers (Yoda *et al.*, 2012). An experimental study has proven that MRAM occupies less area and consumes low power and additionally, non-volatile MRAM memories offers power savings in re-boot and stand by modes.

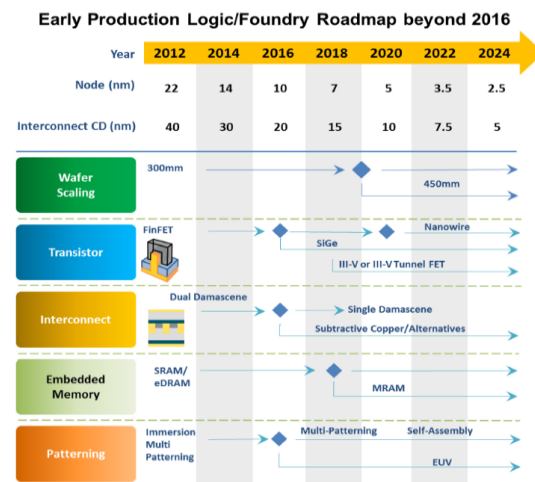


Figure 1. Roadmap of technological development in semiconductor industry (Schuegraf *et al.*, 2013)

The final phase of the manufacturing roadmap includes patterning. The main challenge faced while working on patterning is the availability of high-end and highly productive lithography techniques. Direct patterning, is the traditional single patterning followed by an etching pattern, which is replaced by the multi-patterning technique. Multi patterning technique is complex and causes severe layout restrictions. Extreme Ultra Lithography (EUV) holds significant importance in the industry. Alternatives to this technique for this technique are

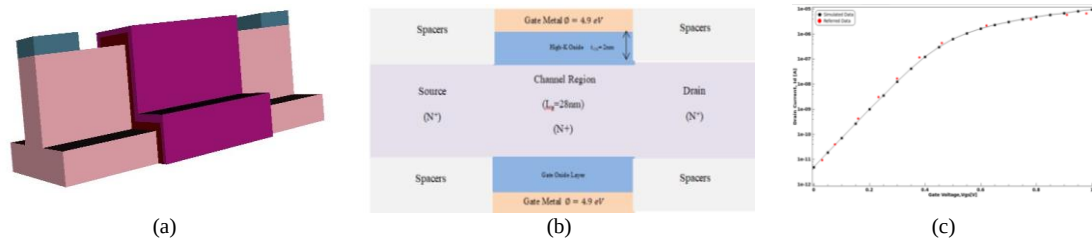


Figure 2. (a) 3D view of IT Junctionless Transistor without oxide isolation (b) 2D Schematic of device (c) Match Id-V_{gs} Characteristics with experimental data in (Paz *et al.*, 2015)

Table 1. Dimensions of different region of designed device

Parameter	ITJLFET
Gate Length	14 nm, 18 nm, 22 nm, and 30 nm
Doping (N_D)	$5 \times 10^{17} \text{cm}^{-3}$, $1 \times 10^{18} \text{cm}^{-3}$, $5 \times 10^{18} \text{cm}^{-3}$, and $1 \times 10^{19} \text{cm}^{-3}$
EOT of Gate Oxide	1 nm and 2 nm
Work Function	4.7 to 5.0 eV
Spacers (L_s and L_d)	11 nm
Spacer Dielectric	SiO_2
UTB	5 nm
Energy Gap	1.1 eV
Temperature	250 K, 275 K, 300 K, and 350 K
Drain Supply Voltage	0.05 V and 1 V

under discovery, and self-assembly and 3D vertical nanowires are among the consideration for these alternatives (Ma *et al.*, 2011).

These aforementioned branches are part of the technology roadmap and provide designers with the flexibility to find the optimal solution. Given the long-term nature of investments in manufacturing, it is essential to build confidence before adopting and implementing new manufacturing methods. Solutions are required to be developed which are consistent with Moore's Law and therefore, meet the design rule boundary conditions (Jeon, 2020; Kumar and Kumar, 2021b).

Device Structure and Simulation Framework

The inverted-T junctionless FET (ITJLFET) structure is created and simulated through the Visual TCAD with Genius 3D device simulator by Cogenda (2008). Visual TCAD can perform 2D as well as 3D simulation. In addition to that, it is capable of performing circuit simulation and mixed circuit/device simulation. The designed structure of inverted-T junctionless FET is depicted in Figure 2(a) and the 2D schematic of the proposed device is shown in Figure 2(b). To investigate the electrical parameters of ITJLFET, various process and geometric parameters are varied. The designed ITJLFET has a gate length (L_g) 30 nm, a width of

a silicon nanowire (W_{si}) is 10 nm, a height of a silicon nanowire (H_{si}) is 15 nm and UTB thickness is 5 nm. In junctionless FET, there is no doping gradient so a uniform doping concentration of $1 \times 10^{19} \text{cm}^{-3}$ is maintained from source to drain. The equivalent oxide thickness (EOT) at the interface is calculated using Equation 1.

$$EOT = T_{\text{SiO}_2} + (T_{\text{high-k}} * 3.9) / (\text{high} - K) \quad (1)$$

Where 'k' is the permittivity of used high-K dielectric, $T_{\text{high-k}}$ is the thickness of high-k dielectric and T_{SiO_2} is the effective SiO_2 thickness (Cheng *et al.*, 1999).

The high-k gate oxide HfO_2 of 2 nm is considered to have high electrostatic integrity. A spacer length of 11 nm is considered between source-gate and gate-drain terminals to achieve higher immunity against subthreshold behaviour. The device models and parameters for the junctionless transistor are calibrated by comparing with the experimental data. Figure 2(c) represents the calibration of simulation results against the calibrated data in (Paz *et al.*, 2015). The parameters taken into consideration while designing junctionless FET are listed in Table 1.

While simulating the designed device various physical models were taken into accounts i.e. Lombardi mobility model is incorporated to get insight of scattering phenomena like surface

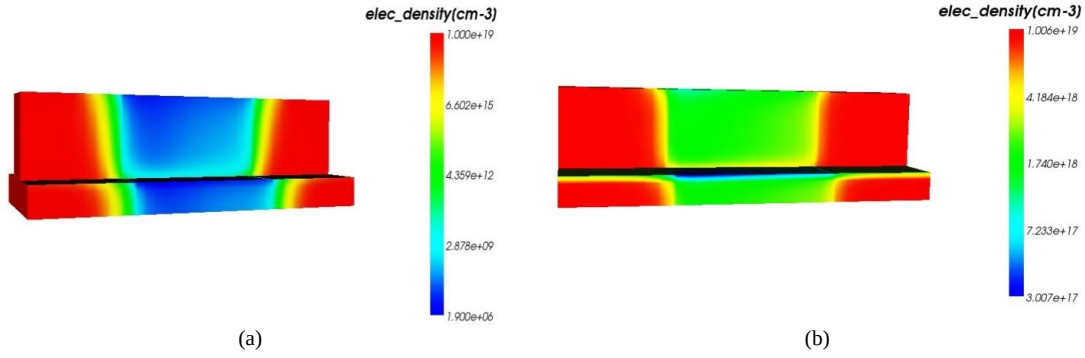


Figure 3. (a) Simulated Device when channel is depleted, (b) when channel is conducting

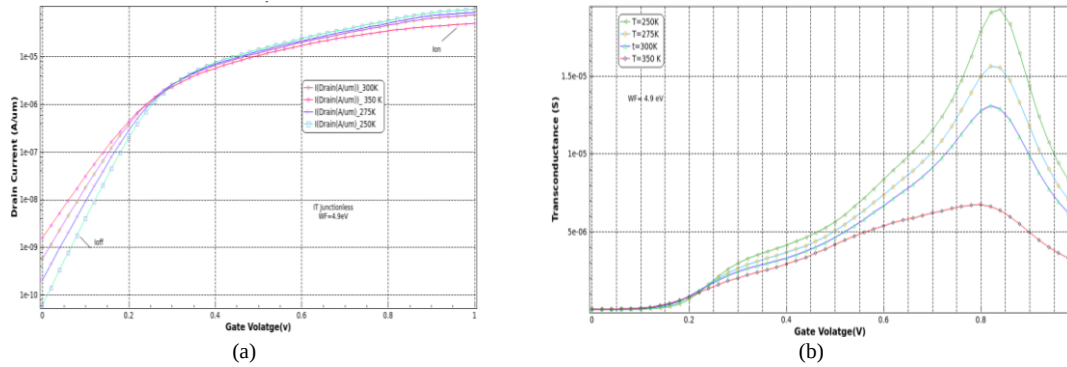


Figure 4. (a) I_d - V_g Characteristics at different temperature (b) Transconductance measurement at different temperature

Table 2. Analog and Short channel performance of IT Junctionless transistor at different temperature

Temp. (K)	DIBL (mV/V)	SS (mV/dec)	I_{ON} (μA)	I_{OFF} (A)	I_{ON}/I_{OFF}	$g_{m,max}$ (μS)	C_{gg} (aF)	f_T (THz)	TGF (V^{-1})
250	29.871	54.48	6.892	4.277×10^{-12}	1.611×10^6	19.06	22.04	1.12	66.44
275	31.11	60.15	5.919	3.915×10^{-11}	1.512×10^5	15.6	24.14	0.92	57.52
300	32.64	65.89	5.212	1.419×10^{-11}	3.673×10^5	13.07	26.78	0.77	50.58
350	29.69	75.711	3.445	1.078×10^{-10}	3.191×10^4	6.71	34.59	0.31	41.86

roughness and acoustic phonons. As IT junctionless FETs are heavily doped, Bandgap narrowing and Fermi Dirac distribution models are considered. To investigate the recombination and generation phenomena SRH recombination model is depleted. Density gradient model taken into account to check for quantum effects in inversion layer. Figure 3(a) represents the simulated device before channel formation and Figure 3(b) represents the device after the channel is formed. The threshold voltage (V_{th}) is extorted using constant current method at drain current given in Equation 2

$$I_D = 100 \text{ nA} \times (W_{eff}/L_G) \quad (2)$$

where L_G is the length of the gate and W_{eff} is effective device width.

Simulation Results and Discussion

To investigate the performance, various factors were taken into account namely work function, Temperature, doping concentration, and gate oxide dielectric. Simulations have been performed to observe and evaluate the parameters that affect the performance of IT junctionless transistors at nanoscale dimensions. For different parametric variations, parameters like I_{ON} , I_{OFF} , DIBL, SS (subthreshold swing), G_m , TGF and C_{gg} , etc. has been evaluated and discussed.

Temperature Variations

The I_d and V_g plot for IT junctionless FET is illustrated in Figure 4(a). The device characteristics are shown at the log scale at different temperatures.

When the applied value of V_{GS} is 0.25 V the variation in temperature is insignificant i.e. Temperature Coefficient (TC) is zero. It has been observed that a rise in temperature leads to a rise in leakage current but there is a marginal effect on the on-state current as shown in Table 2. The increase in temperature breaks the silicon lattice bonds which generate the electron-hole pairs and results in an increase of diffusion drain current. Also, mobility degrades due to diffusion beyond room temperature which further reduces the drain current. From Table 2, it can be seen that with the rise in temperature, leakage current increases and I_{ON} will remain almost constant. The high I_{ON}/I_{OFF} ratio is observed at a lower temperature due to decreased off-state leakage current.

There is increase in leakage current due to SRH recombinations and higher diffusion current which greatly rely on temperature. The intrinsic concentration and temperature are related mathematically as

$$n_i = \exp(-E_g/2\sigma T) \quad (3)$$

where ‘ σ ’ is the Boltzman constant, E_g represents the energy gap and ‘ T ’ is the temperature (Vadthiya and Mishra, 2015). As the channel is heavily doped in junctionless transistors, ionized scattering and lattice scattering controls the mobility. As a result, scattering compensates each other, and the mobility of carriers becomes independent of temperature.

The DIBL and SS evaluate the device efficiency in the subthreshold region and are calculated using Equations (4) and (5) (Vadthiya and Mishra, 2015):

$$\text{DIBL (mV/V)} = \frac{V_{th1} - V_{th2}}{V_{DS1} - V_{DS2}} \quad (4)$$

$$\text{SS (mV/dec)} = \left[\frac{\partial \log_{10}(I_D)}{\partial V_{GS}} \right]^{-1} \quad (5)$$

where V_{th1} is procured at V_{DS1} of 0.05 V and V_{th2} is procured at V_{DS2} of 1V. I_D is the drain current and V_{GS} represents the gate source voltage.

Table 2 represents the parameters measured at different temperatures. Figures 4(b) and 5(b) represents the transconductance and transconductance generation factor (TGF) of IT junctionless transistor at different temperatures.

TGF indicates how efficiently the device converts the DC power into AC frequency. Higher g_m indicates the device will have higher TGF which leads to the better analog performance of the device. The transconductance (g_m) and transconductance generation factor (TGF) are vital parameter in implementing operational amplifiers and has been

calculated at various temperatures. The TGF is measured as

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \quad (6)$$

$$\text{TGF} = g_m / I_D \quad (7)$$

where g_m is the transconductance of the device and I_D represents the drain current. At low temperatures, TGF value is observed to be higher due to an increase in g_m value (Vadthiya and Mishra, 2015).

Performance Measurement

Device Characteristics Analysis

JL transistor is a highly flexible device in terms of V_{th} . Fluctuations in the threshold voltage (V_{th}) can be caused by various factors such as W_{si} , doping concentrations, random dopant fluctuations (RDF), and work function difference, etc. In UTB devices, metal gates with high work function are used to control short channel effects. This work explores the device characteristics by varying doping concentration, temperature, work function, and dielectric constant.

Analog Performance Investigation

As transistors feature size is scaled down, more transistors can be placed on a single chip which directs to the idea of system-on-chip (SOC). This enhances the performance, especially in terms of speed. This integration includes analog/RF circuits with digital and memory circuits on a single chip, making it necessary to inspect device performance for analog and RF applications. The device to be utilized for high-frequency applications should have low parasitics since parasitic capacitance establishes the link between the input and output node. Also, parasitic capacitance influences the speed of operation and power dissipation.

The gate capacitance (C_{gg}) is the combination of capacitance from source to drain terminals and is used to evaluate various parameters such as cut-off frequency (f_T) and delay (τ). The graph for C_{gg} at different temperatures is shown in Figure 5(a). From the obtained results it is perceived that with the rise in temperature the value of gate capacitance increases due to lowering of the energy bandgap which further degrades the energy barrier and results in an increase of charge carrier along the channel. As the charge carrier increases in the channel under gate region leads to an increase in the gate capacitance. The cut-off frequency is obtained using Equation (8).

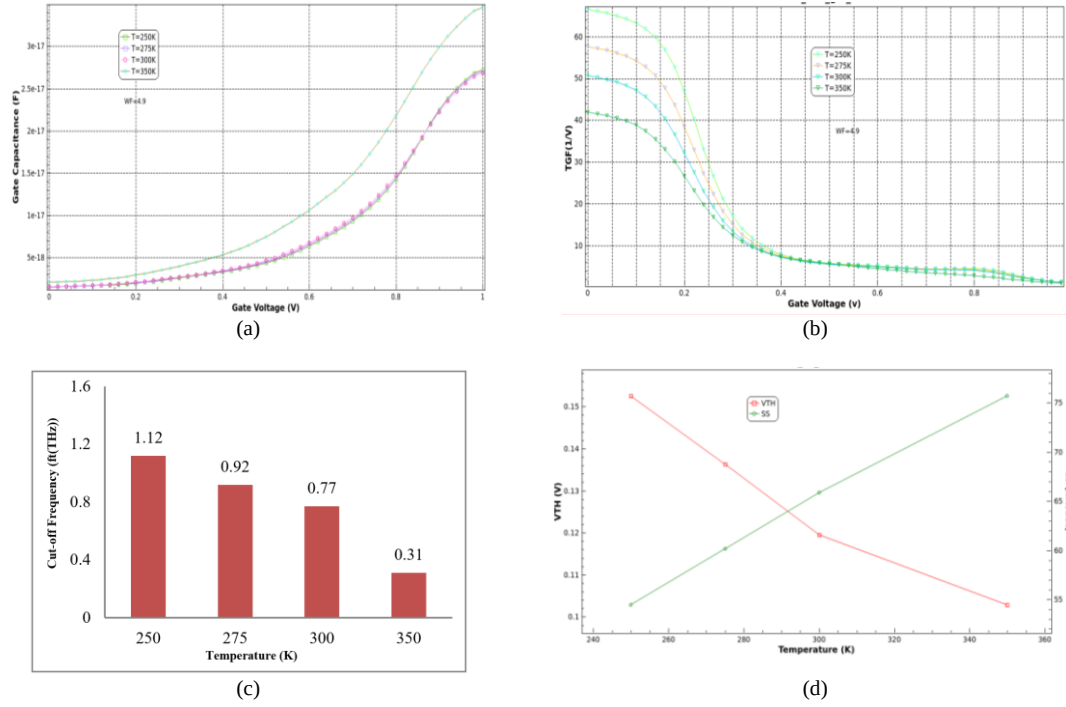


Figure 5. IT Junctionless FET characteristics (a) Gate Capacitance (C_{gg}) (b) Transconductance generation factor (TGF) (c) Frequency variation with respect to temperature (d) Threshold and Subthreshold Swing trade off

Table 3. Analog and Short channel performance of IT Junctionless transistor at different doping concentrations

N_D (cm^{-3})	DIBL (mV/V)	SS (mV/dec)	I_{ON} (μA)	I_{OFF} (A)	I_{ON}/I_{OFF}	$g_{m,max}$ (μS)	C_{gg} (aF)
5×10^{17}	20.83	62.17	1.314	1.929×10^{-17}	1.226×10^{12}	5.05	14.9
1×10^{18}	22.27	62.34	3.741	1.167×10^{-17}	4.041×10^{11}	5.37	19.6
5×10^{18}	26.22	63.18	4.178	2.645×10^{-15}	8.791×10^{10}	13.4	25.6
1×10^{19}	32.64	65.89	5.212	1.419×10^{-11}	6.123×10^9	13.1	26.78

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (8)$$

Where C_{gg} is the total gate capacitance and g_m is the transconductance of the device. As temperature increases, the cut-off frequency decreases as seen in (Vadthiya *et al.*, 2020). The change in frequency is due to variations in g_m and C_{gg} , as they have equal and opposite effect on the cut-off frequency of the device. The variation of the cut-off frequency w.r.t to gate voltage at different temperature is illustrated in the Figure 5(c). Further, the threshold voltage is the crucial factor that indicates a device's ability to change from off-state to on state and achieving it at low V_{GS} is desirable. Figure 5(d) shows that there is decrease in V_{th} value and an increase in SS value, with increase in temperature. At lower temperatures, as the value of SS is reduced it means the device will be turned

on faster and hence can be used for high-switching applications.

Impact of Doping and Work Function

The doping variations of junctionless FET are evaluated at work function 4.9 eV, V_{GS} is swept from 0 to 1 V and $V_{DS} = 0.05$ V and 1 V. The variation in I_d - V_{GS} due to doping variations is illustrated in Figure 6(a). It has been observed that as doping concentration increases I_{on} as well as I_{off} increases. Lower doping concentration has enhanced subthreshold leakage performance but I_{ON} reduces at lower doping levels. At a concentration of $1 \times 10^{19} / \text{cm}^3$ the device exhibits higher I_{ON} current and lowest value of threshold voltage, making suitable for low power applications. However, increasing doping levels may affect mobility due to high scattering rates. Table 3 represents the impact of variations in doping concentration on IT

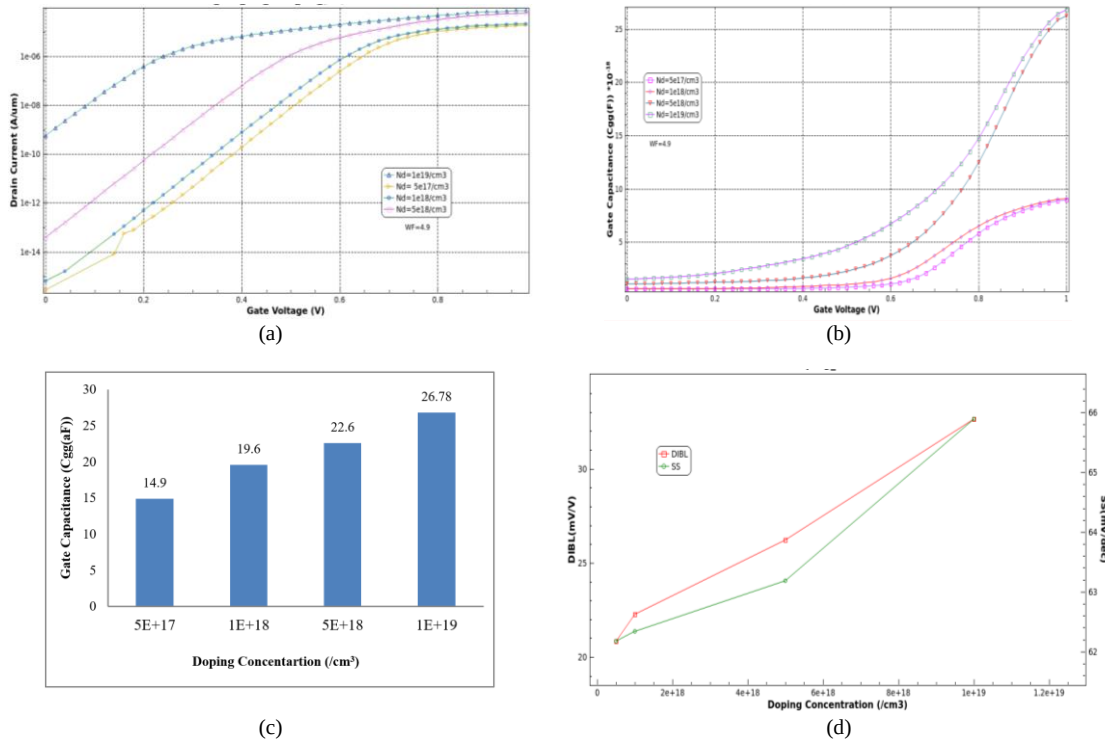


Figure 6. IT Junctionless FET characteristics (a) Doping Variation (b) Gate capacitance (C_{gg}) (c) Gate capacitance variation with increasing doping (d) SS and DIBL variation with doping Concentration

Table 4. Analog and Short channel performance of IT Junctionless transistor at different work function

ϕ_m	DIBL (mV/V)	SS (mV/dec)	V_{th} (V)	I_{ON} (μA)	I_{OFF} (A)	I_{ON}/I_{OFF}	$g_{m,max}$ (μS)	C_{gg} (aF)
4.7	27.31	66.57	0.035	6.306	6.835×10^{-8}	9.226×10^1	13.01	30.67
4.8	39.22	64.63	0.0807	6.588	1.375×10^{-9}	4.791×10^3	12.89	29.29
4.9	32.64	65.89	0.11	5.212	1.419×10^{-11}	3.67×10^5	13.07	26.78
5.0	32.64	64.74	0.22	2.422	1.141×10^{-12}	2.123×10^6	12.51	21.5

junctionless FET. Figure 6(b) represents the gate capacitance (C_{gg}) w.r.t to gate voltage at different doping levels and Figure 6(c) shows the exact value of gate capacitance at different doping levels. It has been observed that there is increase in the gate capacitance with increase in the doping levels. An increase of the doping introduces more charge carriers into the semiconductor material, hence, there is increase in overall charge. This leads to increase in capacitance, as capacitance is directly proportional to charge. The variation in the DIBL and SS with change in doping concentration is shown in Figure 6(d). There is increase in DIBL and SS as doping concentration increases. Additionally, increase in doping concentration leads to lower mobility due to enhance coulomb scattering rates (Park and Choi, 2012). There is reduction of the bandgap energy due to increase in doping levels which may leads to the high impact ionization rate.

The work function is varied from 4.7 to 5.0 eV at constant doping of $1 \times 10^{19}/\text{cm}^3$ and temperature 300 K. The increase in work function leads to a decrease in leakage current and at the same time increases the threshold voltage. The device characteristics of work function variation are shown in Figure 7(a). Therefore, from observations, it is visible that the higher value of the gate work function makes the channel fully depleted quickly and shows improved performance in the OFF state. Table 4 represents the impact of work function variations on IT junctionless transistor. It has been noticed that increase in work function results in a decrease in off-state leakage current and also shows a reduction in the on-state current. When the work function of gate increases, there is decrease in the gate-to-channel concentration. This leads to reduction in leakage current from gate to source and drain. But with enhanced performance in

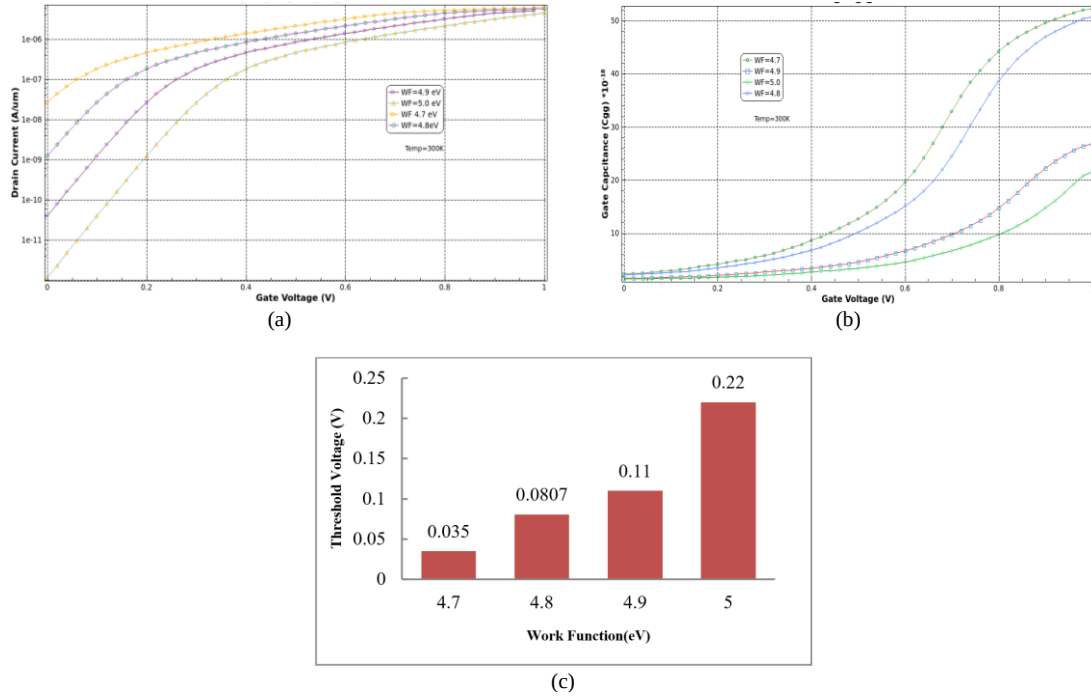


Figure 7. IT Junctionless FET characteristics, (a) Work Function Variation, (b) Gate capacitance (C_{gg}), (c) Threshold Voltage Variation with increasing work function

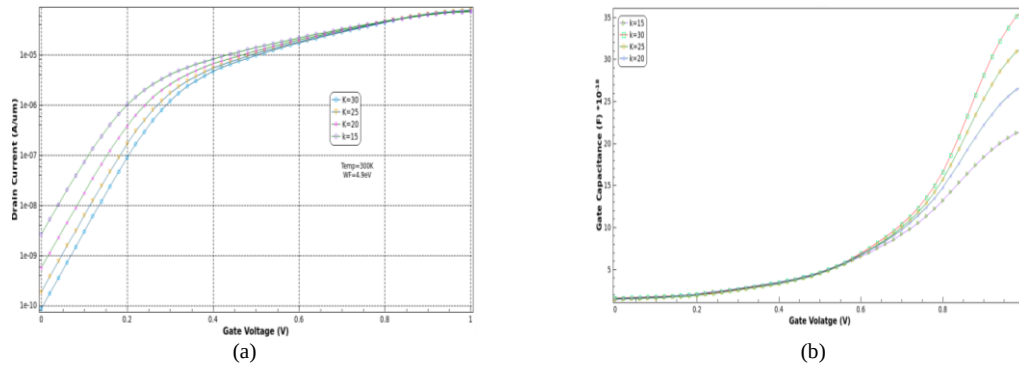


Figure 8. IT Junctionless FET characteristics, (a) Dielectric Variation Variation, (b) Gate capacitance (C_{gg})

an off-state, the device requires more time to turn off as there is a decrease in the threshold voltage which impacts the SS. Figure 7(c) shows the reduction in threshold voltage with increased metal gate work function. Figure 7(b) represents gate capacitance variation w.r.t to gate voltage at different work function. It has been observed that with increase in metal gate work function there is increase in the gate capacitance.

Impact of Dielectric Constant

To determine how oxide dielectric affects the conductivity of the channel, the permittivity of oxide is being experimented on over different points

(15, 20, 25, and 30). To investigate the effect device is simulated by keeping the doping concentration constant $N_d = 1 \times 10^{19}/\text{cm}^3$ and work function is set to 4.9 eV.

When permittivity of oxide capacitance is varied it has been observed that as the permittivity is increased there is a reduction in off-state current as high value of dielectric provides better insulation and reduces the tunnelling of charge carriers. Figure 8(a) represents the I_d - V_{gs} characteristics at different dielectric constant for IT junctionless transistors. The results of varying dielectric constant are listed in Table 5. An increase in dielectric constant shows enhanced performance in the off-state. Figure 8(b)

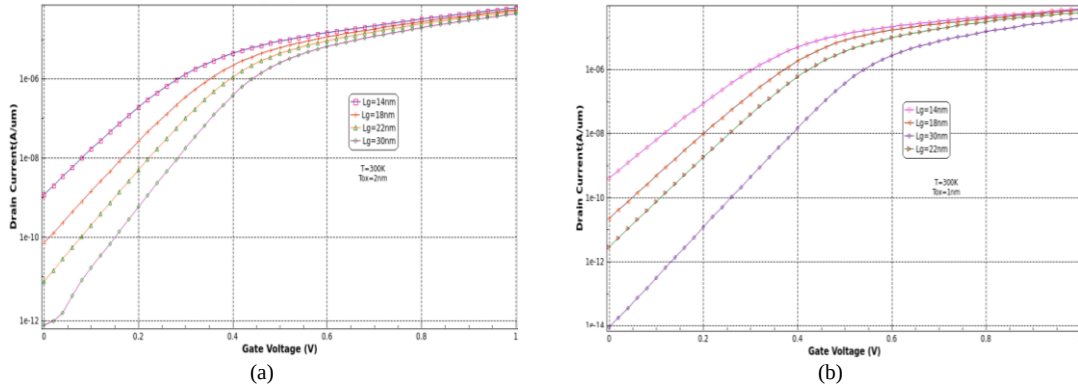


Figure 9. (a) Channel Variations at 2 nm oxide thickness (b) Channel Variations at 1 nm oxide thickness

Table 5. Analog and Short channel performance of IT Junctionless transistor at different permittivities

Dielectric Constant (K)	DIBL (mV/V)	SS (mV/dec)	I_{ON} (μA)	I_{OFF} (A)	I_{ON}/I_{OFF}	$g_{m,max}$ (μS)	C_{gg} (aF)
15	35.68	67.55	5.108	1.843×10^{-10}	2.77×10^4	11.7	21.47
20	32.64	65.89	5.919	1.419×10^{-11}	4.17×10^5	13.07	26.78
25	29.67	64.84	5.319	1.275×10^{-11}	4.18×10^5	14.17	31.39
30	28.55	64.38	5.37	5.953×10^{-12}	9.02×10^6	14.91	35.7

Table 6 Analog and Short channel performance of IT Junctionless transistor at different channel length

L_g (nm)	DIBL (mV/V)	SS (mV/dec)	V_{th} (V)	I_{ON} (μA)	I_{OFF} (A)
14	170	84.62	0.15	4.309	8.01×10^{-11}
18	120	75.10	0.22	3.9	4.743×10^{-12}
22	85	69.65	0.27	3.63	5.141×10^{-13}
30	47	64.42	0.32	3.18	3.213×10^{-14}

represents the gate capacitance (C_{gg}) w.r.t to gate voltage at different gate oxide dielectric. As Oxide capacitance increases, there is increase in the gate capacitance as C_{ox} is directly proportional to ϵ_{ox} given by Equation 9:

$$C_{ox} = \epsilon_{ox} / T_{ox} \quad (9)$$

where ϵ_{ox} is the permittivity of the gate oxide material and T_{ox} is the thickness of gate oxide.

Channel Length Variations and Oxide Thickness

In order to investigate the performance through the geometric variations, channel length is varied from 14 nm to 30 nm. The results are presented in Table 6. The ITJLFET is calibrated at different channel lengths and obtained results demonstrates that as transistor is scaled down, it performs better in terms of SS slope but DIBL increases drastically. Reduction in gate length increases the leakage current and leads to decrease of switching current ratios. High value of metal gate work function is required at small channel length to make it completely deplete of charge carriers and

all the simulations are carried out at 5.1 eV work function. Moreover, the oxide thickness is varied from 1 nm to 2 nm and obtained results are shown in Figures 9(a) and 9(b). Thinning of oxide thickness is preferred at reduced channel length due to decreased threshold voltage roll-off. But thin oxide may result in increased leakage current due to tunnelling of carriers. There exists a trade-off about suppressing the SCE's without increasing the off state leakage current at reduced gate oxide thickness.

Comparison of Transfer Characteristics

In the present work, Inverted-T junctionless transistor and conventional JLFET is designed at 30-nm technology node. Junctionless transistors are known to be ON devices and can be off by supplying sufficient amount of metal work function between the gate metal and the channel material. For JLFET and ITJLFET to have similar value of the threshold voltage (V_{th}), the ϕ_{ms} requirement for ITJLFET is more as compared to JLFET because UTB in ITJLFET get turned on early in contrast to fin transistor (Fahad *et al.*, 2015). It has been witnessed

that off state leakage is almost same for ITJLFET as compared to conventional JFET. Moreover, it shows the improvement in on-state current of about 64%.

Conclusions

The ITJLFT is designed at different gate lengths ranging from 14 nm to 30 nm. The performance is measured by process and geometric variations. The temperature dependence of the inverted-T junctionless transistor is being carried out and it has been observed that temperature has less effect on transconductance (g_m), gate capacitance (C_{gg}), TGF, and cut-off frequency. Also, the effect of other process parameter variations is investigated and it is noticed that ITJFET performs better in the 4.8 to 4.9 eV work function range due to moderate ON-OFF characteristics. At $1 \times 10^{19} \text{ cm}^{-3}$ doping, it shows improved I_{ON} drain current and short channel performance. The gate length is varied from 14 nm to 30 nm and it has been observed that at reduced channel length off state leakage current increases and there is decrease in threshold voltage. It exhibits enhanced gate electrostatics at higher gate length (L_g). Also, there exists a trade-off about controlling the SCE's without increasing the off state leakage current when gate oxide thickness is reduced.

The device has improved on-state current of 64% in comparison to the conventional JLFET. The device has the cut-off frequency in the range of the THz. Hence device can be used for high frequency applications such as microwave and radar communication systems. But, as the device area increases it leads to increase in the threshold voltage as compared to JLFET.

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References

Agnihotri, P. and Tripathi, N. (2019). Junctionless transistors for future applications. *International Journal of Information Technology and Electrical Engineering*, 8(4):50-53. <https://doi.org/10.13140/RG.2.2.32152.88322>.

- Andricacos, P.C., Uzoh, C., Dukovic J.O., Horkans, J., and Deligianni, H. (1998). Damascene copper electroplating for chip interconnections. *IBM Journal of Research and Development*, 42(5):567-574. <https://doi.org/10.1147/rd.425.0567>
- Bagga, N., Kumar, A., Bhattacharjee, A., and Dasgupta, S. (2017). Performance evaluation of a novel GAA schottky junction (GAASJ) TFET with heavily doped pocket. *Superlattices and Microstructure*, 109:545-552. <https://doi.org/10.1016/j.spmi.2017.05.040>
- Bashir, M.Y., Raushan, M.A., Ahmad, S., and Siddiqui M.J. (2022). Investigation of gate material engineering in junctionless transistor for digital and analog applications. *Silicon*, 14:2851-2862. <https://doi.org/10.1007/s12633-021-01066-8>
- Bharath, S.V. and Narendar, V. (2021). Design and deep insights into Sub-10 nm spacer engineered junctionless FinFET for nanoscale applications. *ECS Journal of Solid State Science and Technology*, 10:013008. <https://doi.org/10.1149/2162-8777/abddd4>
- Bhuyan, M.H. (2017). History and evolution of CMOS technology and its application in semiconductor industry. *SEU Journal of Science and Engineering*, 11(1):30-42.
- Bohr, M.T. (1995). Interconnect scaling-the real limiter to high performance ULSI. In: *Proceedings of International Electron Devices Meeting*, p. 241-244. <https://doi.org/10.1109/IEDM.1995.499187>
- Cheng, B., Cao, M., Rao, R., Inani, A., Vande Voorde, P., Greene, W.M., Stork, J.M.C., Zhiping, Y., Zeitsoff, P.M., and Woo, J.C.S. (1999). The impact of high-k gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs. *IEEE Transactions on Electron Devices*, 46(7):1537-1544. <https://doi.org/10.1109/16.772508>
- Choi, S.J., Moon, D.I., Kim, S., Duarte, J.P., and Choi, Y.K. (2011). Sensitivity of threshold voltage to nanowire width variation in junctionless transistors. *IEEE Electron Device Letters*, 32(2):125-127. <https://doi.org/10.1109/LED.2010.2093506>
- Cogenda Pvt Ltd. (2008). Singapore, Genius, 3-D Device Simulator, Version 1.9.3, Reference Manual, Singapore.
- Colinge, J.P. (2012). Junctionless transistors. 2012 IEEE International Meeting for Future of Electron Devices, Kansai, Suita, Japan, p. 1-2, <https://doi.org/10.1109/IMFEDK.2012.6218561>
- Colinge, J.P., Lee, C.W., Afzalian, A., Akhavan, N.D., Yan, R., Ferain, I., Razavi, P., O'Neill, B., Blake, A., White, M., Kelleher, A.M., McCarthy, B., and Murphy, R. (2010). Nanowire transistors without junctions. *Nature Nanotechnology*, 5:225-229. <https://doi.org/10.1038/nnano.2010.15>
- Colinge, J.P., Lee, C.W., Akhavan, N.D., Yan, R., Ferain, I., Razavi, P., Kranti, A., and Yu, R. (2011). Junctionless transistors: physics and properties. *Semiconductor on Insulator Materials and Nanoelectronics Application*, p. 187-200. https://doi.org/10.1007/978-3-642-15868-1_10
- Fahad, H.M., Hu, C., and Hussain, M.M. (2015). Simulation study of a 3-D device integrating FinFET and UTBFET. *IEEE Transactions on Electron Devices*, 62(1):83-87. <https://doi.org/10.1109/TED.2014.2372695>
- International Technology Roadmap for Semiconductors (ITRS). (2015). Semiconductor Industry Association. [Online]. Available: <https://www.semiconductors.org/resources/2015-international-technology-roadmap-for-semiconductors-its/>.
- Jeon, D.Y. (2020). Simple estimation of intrinsic electrical parameters in junctionless transistors. *AIP Advances*, 10(9):095118. <https://doi.org/10.1063/5.0022769>
- Kaushik, B.K., Goel, S., and Rauthan, G. (2007). Future VLSI interconnects: Optical fiber or carbon nanotube - A review. *Microelectronics International*, 24(2):53-56. <https://doi.org/10.1108/13565360710745601>

- Kuhn, K.J., Avci, U., Cappellani, A., Giles, M.D., Haverty, M., Kim, S., Kotlyar, R., Manipatrani, S., Nikonov, D., Pawashe, C., Radosavljevic, M., Rios, R., Shankar, S., Vedula, R., Chaua, R., and Young, I. (2012). The ultimate CMOS device and beyond. In: 2012 International Electron Devices Meeting, San Francisco, USA, p. 8.1.1-8.1.4. <https://doi.org/10.1109/IEDM.2012.6479001>
- Kumar, R. and Kumar, A. (2021a). Hafnium based high-k dielectric gatestacked (GS) gate material engineered (GME) junctionless nanotube MOSFET for digital applications. *Applied Physics A*, 127:26. <https://doi.org/10.1007/s00339-020-04217-7>
- Kumar, R. and Kumar, A. (2021b). Hetro-Dielectric (HD) Oxide-Engineered Junctionless Double Gate all around (DGAA) Nanotube Field Effect Transistor (FET). *Silicon*, 13:2177-2184. <https://doi.org/10.1007/s12633-020-00705-w>
- Lilienfeld, J.E., Inventor; Individual, Current Assignee. 1925. Method and Apparatus for Controlling Electric Currents. U.S. patent no. US1745175A.
- Lilienfeld, J.E., Inventor; Individual, Current Assignee. 1928. Device for Controlling Electric Current Filed. U.S. patent no. US1900018A.
- Ma, Y., Sweis, J., Bencher, C., Deng, Y., Dai, H., Yoshida, H., Gisuthan, B., Kye, J., and Levinson, H. (2011). Double patterning compliant logic design. In: *Proceedings of SPIE - The International Society for Optical Engineering*, San Jose, United States, Volume 7974, <https://doi.org/10.1117/12.879846>
- Matick, R.E. and Schuster, S.E. (2005). Logic-based eDRAM: Origins and rationale for use. *IBM Journal of Research and Development*, 49(1):145-165. <https://doi.org/10.1147/rd.491.0145>
- Moore, G.E. (1965). Cramming more components onto integrated circuits. *Electronics Magazine*, 38:114-117.
- Nelapati, R.P. and K., S. (2020). Process variation study of SELBOX inverted- T junctionless FinFET for high-performance applications. *Silicon*, 12:1699-1706. <https://doi.org/10.1007/s12633-019-00270-x>
- Pal, P.K., Kaushik, B.K., and Dasgupta, S. (2014). Investigation of symmetric dual-k spacer trigate FinFETs from delay perspective. *IEEE Transactions on Electron Devices*, 61(11):3579-3585. <https://doi.org/10.1109/TED.2014.2351616>
- Park, H. and Choi, B. (2012). A study on the performance of metal-oxide-semiconductor-field-effect-transistors with asymmetric junction doping structure. *Current Applied Physics*, 12(6):1503-1509. <https://doi.org/10.1016/j.cap.2012.04.026>
- Paz, B.C., Pavanello, M.A., Cassé, M., Barraud, S., Reimbold, G., Faynot, O., Avila-Herrera, F., and Cerdeira, A. (2015). From double to triple gate: Modeling junctionless nanowire transistors. In: *EUROSOI-ULIS 2015: 2015 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon*, Bologna, Italy, p. 5-8. <https://doi.org/10.1109/ULIS.2015.7063759>
- Sahay, S. and Kumar M.J. (2019a). Fundamentals of junctionless field-effect transistors. In: *Junctionless Field-Effect Transistors: Design, Modeling, and Simulation*, Sahay, S. and Kumar, M.J. (eds.). Wiley Online Library, p. 67-123. <https://doi.org/10.1002/9781119523543.ch3>
- Sahay, S. and Kumar, M.K. (2019b). Introduction to field-effect transistors. In: *Junctionless Field-Effect Transistors: Design, Modeling, and Simulation*, Sahay, S. and Kumar, M.J. (eds.). Wiley Online Library, p. 1-26. <https://doi.org/10.1002/9781119523543.ch1>
- Schuegraf, K., Abraham, M.C., Brand, A., Naik, M., and Thakur, R. (2013). Semiconductor logic technology innovation to achieve sub-10 nm manufacturing. *IEEE Journal of the Electron Devices Society*, 1(3):66-75, <https://doi.org/10.1109/JEDS.2013.2271582>
- Shankar, R., Kaushal, G., Maheshwaram, S., Dasgupta, S., and Manhas, S.K. (2014). A degradation model of double gate and gate-all-around mosfets with interface trapped charges including effects of channel mobile charge carriers. In: *IEEE Transactions on Device and Materials Reliability*, 14(2):689-697. <https://doi.org/10.1109/TDMR.2014.2310292>
- Trevisoli, R.D., Doria, R.T., Souzad, M., and Pavanello, M.A. (2011). Threshold voltage in junctionless nanowire transistors. *Semiconductor Science and Technology*, 21(10):1015009. <https://doi.org/10.1088/0268-1242/26/10/105009>
- Vadthiya, N. and Mishra, R.A. (2015). Analytical modeling and simulation of multigate FinFET devices and the impact of high-k dielectrics on short channel effects (SCEs). *Superlattices and Microstructures*, 85:357-369. <https://doi.org/10.1016/j.spmi.2015.06.004>
- Vadthiya, N., Narware, P., Bheemudu, V., and Sunitha, B. (2020). A novel bottom-spacer ground-plane (BSGP) FinFET for improved logic and analog/RF performance. *AEU - International Journal of Electronics and Communications*, 127:153459. <https://doi.org/10.1016/j.aeeu.2020.153459>
- Vakkalakula, B.S. and Vadthiya, N. (2021). Design and temperature assessment of junctionless nanosheet FET for nanoscale applications. *Silicon*, 14:3823-3834 <https://doi.org/10.1007/s12633-021-01145-w>
- Vandana, B., Das, J.K., Mohapatra, S.K., and Jyothi, M.S. (2017). Impact on gate oxide material of inverted 'T' junctionless FinFET at 22 nm technology node. In: *2017 1st International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech)*, Kolkata, India, p. 1-5. <https://doi.org/10.1109/IEMENTECH.2017.8076957>
- Vandana, B., Patro, B.S., Das, J.K., Kaushik, B.K., and Mohapatra, S.M. (2018). Inverted 'T' junctionless FinFET (ITJL FinFET): performance estimation through device geometry variation. *ECS Journal of Solid States Science and Technology*, 7(4):52-59. <https://doi.org/10.1149/2.0071804jss>
- Wong, H.S.P., Frank, D.J., and Solomon, P.M. (1998). Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation. In: *International Electron Devices Meeting 1998. Technical Digest (Cat. No. 98CH36217)*, San Francisco, CA, USA, p. 407-410. <https://doi.org/10.1109/IEDM.1998.746385>
- Yoda, H., Fujita, S., Shimomura, N., Kitagawa, E., Abe, K., Nomura, K., Noguchi, H., and Ito, J. (2012). Progress of STT-MRAM technology and the effect on normally-off computing systems. 2012 International Electron Devices Meeting, San Francisco, CA, USA, p. 11.3.1-11.3.4. <https://doi.org/10.1109/IEDM.2012.6479023>
- Zhang, W., Fossum, J.G., and Mathew, L. (2006) The ITFET: A novel FinFET-based hybrid device. *IEEE Transactions on Electron Devices*, 53(9):2335-2343. <https://doi.org/10.1109/TED.2006.880813>