

RECENT ADVANCES IN HfO₂-BASED FERROELECTRIC FIELD - EFFECT TRANSISTORS: MATERIALS, INTERFACES, ARCHITECTURES, AND RELIABILITY - A REVIEW

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Abstract

HfO₂-based ferroelectric field-effect transistors have emerged as promising candidates for scalable, CMOS-compatible non-volatile memory devices. This review provides an overview of recent progress in the field, highlighting advances in materials, processing, and device engineering. Studies on doped and undoped HfO₂ thin films are surveyed, with comparisons of deposition methods such as atomic layer deposition and sputtering, as well as dopant strategies and interface engineering approaches. The influence of processing parameters, annealing conditions, and electrode choice on the stabilization of metastable orthorhombic phases and resulting ferroelectric properties is critically analyzed. While significant improvements in polarization, switching speed, and endurance have been achieved, challenges such as wake-up and fatigue effects, defect-induced degradation, and maintaining uniform performance at sub-10 nm dimensions remain unresolved. Importantly, interface and electrode engineering are shown to play key roles in enhancing device retention and endurance. By summarizing both the successes and persistent challenges, this review provides a succinct reference for researchers and highlights potential future directions, including 3D integration, variability control, and applications in neuromorphic computing.

Keywords: HfO₂; FeFET; Endurance; Polarization; Computing

Introduction

Moore's Law, which governs the constant development of semiconductor devices, has greatly increased system complexity, integration density, and processing power (Colombo *et al.*, 2024). However, at sub-10 nm nodes, conventional memory technologies like DRAM and Flash are getting close to their basic physical boundaries (Worledge and Hu, 2024). Despite being

quick and scalable, DRAM uses a lot of power because of its volatility and frequent refresh needs (Bhati *et al.*, 2015). However essentially non-volatile, flash memory has drawbacks that make it difficult to integrate with logic processes, such as high write latency, limited durability, and intricate charge-trapping systems (Kim *et al.*, 2023). The semiconductor industry is investigating new

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memory technologies that provide high speed and non-volatility in order to get around these restrictions. One of the most promising of these is the ferroelectric field-effect transistor (FeFET) based on hafnium oxide (HfO_2) (Lehninger *et al.*, 2025). FeFETs are completely compatible with CMOS fabrication and combine quick switching, low power consumption, and non-volatile data retention (Khan *et al.*, 2020). In addition to this, they can be used in next-generation applications such as neuromorphic computing, embedded memory, and compute-in-memory (CIM) (Katehi *et al.*, 2025). The field of ferroelectric materials was revolutionized in 2011 when Wang *et al.* discovered ferroelectricity in doped HfO_2 films (Wang *et al.*, 2025a). HfO_2 has improved thermal stability, high dielectric characteristics, and can be formed using atomic layer deposition (ALD), a technique already used in advanced logic nodes, in contrast to conventional perovskite-based ferroelectrics like PZT and SBT, which have thermal and integration issues (Banerjee *et al.*, 2022). Ferroelectricity in HfO_2 arises from the stabilization of a metastable, non-centrosymmetric orthorhombic phase ($\text{Pca}2_1$). This phase is promoted through doping (e.g., with Si, Zr, Y, Al, or Gd), interfacial control, and post-deposition annealing (Park *et al.*, 2015).

In FeFETs, a ferroelectric HfO_2 layer is integrated into the gate stack of a MOSFET (Cheema *et al.*, 2022). Applying a programming voltage switches the polarization direction of the ferroelectric layer, shifting the channel's threshold voltage (V_{th}) and enabling non-volatile data storage (Chai *et al.*, 2020). These devices demonstrate sub-nanosecond switching speeds, low operating voltages, high endurance ($>10^9$ cycles), and simple one-transistor (1T) cell structures (Choi *et al.*, 2024). Crucially, they offer seamless integration into advanced transistor architectures like FinFETs, nanosheet FETs, and gate-all-around (GAA) designs (Paul *et al.*, 2025). Despite their advantages, FeFETs face critical reliability challenges. Retention loss, endurance degradation, and variability are driven by mechanisms such as charge trapping, domain pinning, and unwanted phase transitions (Thomann and Amrouch, 2023). The ferroelectric orthorhombic phase is inherently metastable and sensitive to scaling and thermal budgets. Interface engineering is also crucial, electrode materials and interfacial layers affect polarization, defect generation, and electrical performance (Wang *et al.*, 2025b). Key reliability concerns include the wake-up effect (initial cycling-induced polarization increase), imprint (built-in field-induced bias), and cycle-to-cycle variability (Jang *et al.*, 2024).

This review highlights recent advances in material processing (ALD, sputtering), electrode selection, and architectural integration. Furthermore, it explores FeFET applications beyond traditional memory, including edge AI, neuromorphic systems, and analog computing, where their non-volatility and analog behavior could revolutionize logic-memory fusion and beyond-von Neumann computing paradigms.

Fundamentals of Ferroelectricity in HfO_2

The discovery of ferroelectricity in doped HfO_2 has challenged traditional views in ferroelectric materials science, particularly regarding the limitations of thin-film ferroelectrics (Schroeder *et al.*, 2022). Unlike classical perovskite ferroelectrics, HfO_2 -based films exhibit robust polarization at nanoscale thicknesses, offering improved scalability, endurance, and integration with CMOS platforms (Jha, 2025). This section outlines the core mechanisms that enable ferroelectricity in HfO_2 , focusing on crystallographic phases, polarization dynamics, doping, and processing effects.

Crystallographic Phases of HfO_2

Pure HfO_2 naturally adopts a centrosymmetric monoclinic phase ($\text{P}2_1/\text{c}$), which is non-ferroelectric as shown in Figure 1. With increasing temperature, it transitions to tetragonal and cubic phases, both paraelectric. The monoclinic ($\text{P}2_1/\text{c}$) phase of hafnium oxide (HfO_2) is stable at room temperature and changes into tetragonal ($\text{P}4_2/\text{nmc}$) and cubic phases at higher temperatures. Remarkably, metastable polar phases, mainly the orthorhombic $\text{Pca}2_1$, coupled with $\text{Pmn}2_1$, $\text{R}3\text{m}$, and $\text{R}3$ structures, are the source of ferroelectricity in HfO_2 thin films. Precise experimental phase identification and characterisation are made more difficult by the coexistence of these polar and nonpolar phases, which are caused by strain, dopants, and size effects. Ferroelectric behavior arises from the stabilization of the metastable, non-centrosymmetric orthorhombic $\text{Pca}2_1$ phase (Jha *et al.*, 2020). This phase features spontaneous polarization driven by asymmetric displacement of Hf^{4+} ions in distorted oxygen octahedra. Unlike perovskites that rely on B-site cation displacement, polarization in HfO_2 is enabled through lattice distortion and unit cell tilting (Zhao *et al.*, 2022).

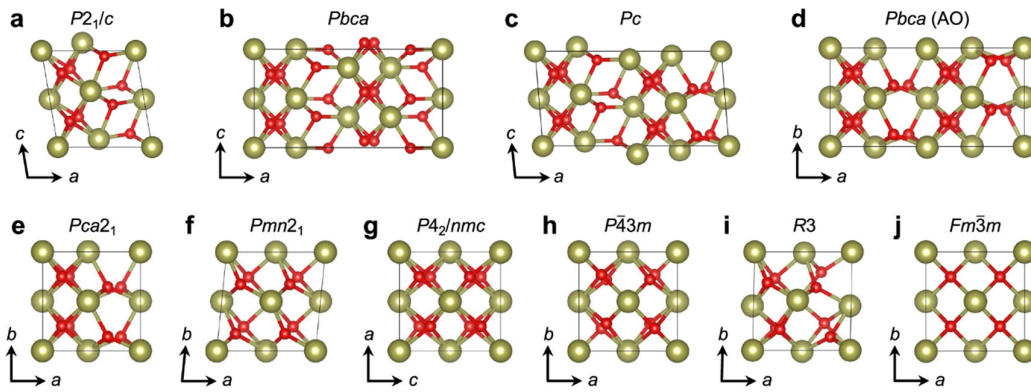


Figure 1. The Hf and O atoms are denoted by golden and red spheres, respectively. a. Nonpolar monoclinic $P2_1/c$. b. Nonpolar orthorhombic $Pbca$. c. Polar monoclinic Pc . d. Antipolar orthorhombic (AO) $Pbca$. e. Polar orthorhombic $Pca2_1$. f. Polar orthorhombic $Pmn2_1$. g. Nonpolar tetragonal $P4_2/nmc$. h. Nonpolar cubic $P4_3m$. i. Polar rhombohedral $R3$. j. Nonpolar cubic $Fm\bar{3}m$. reproduced from (Zhu *et al.*, 2024) under CC-4 license

Mechanism of Polarization

The $Pca2_1$ phase supports reversible polarization, evidenced by a characteristic hysteresis loop in the polarization-electric field (P-E) plot. Switching occurs via nucleation and growth of oppositely polarized domains, primarily through 180° domain wall motion. Depending on conditions like film thickness and interface quality, switching may follow nucleation-limited or domain-wall creep models. Techniques like piezoresponse force microscopy (PFM) and transmission electron microscopy (TEM) confirm nanoscale domain structures and switching pathways. Remanent polarization (P_r) values of $10\text{--}30\ \mu\text{C}/\text{cm}^2$ have been achieved, even in ultrathin films ($\sim 5\text{--}10\ \text{nm}$), supporting HfO_2 's scalability (Sun *et al.*, 2024).

Role of Doping

By stabilizing the non-centrosymmetric orthorhombic phase that gives HfO_2 its ferroelectric activity, doping is essential for promoting and strengthening ferroelectricity. In order to suppress the stable monoclinic phase and encourage the formation of the metastable ferroelectric phase, dopants like aluminum, gadolinium, yttrium, lanthanum, and cerium inject or control oxygen vacancies and mechanical stress (Hoffmann *et al.*, 2015). Dopant type and concentration are crucial: excessive doping prevents the phase transition, whereas an ideal doping range stabilizes ferroelectricity and increases remanent polarization. Additionally, by balancing charge and lowering defects, co-doping with both acceptor and donor dopants can enhance polarization switching and device reliability. Because doping affects phase stability, polarization strength, and structural flaws,

it is crucial to utilize the special ferroelectric properties of HfO_2 thin films for applications in memory devices and microelectronics. Because of this, doped HfO_2 is a promising material that works well with the silicon technology platforms of today.

Thickness and Size Effects

Ferroelectricity in HfO_2 persists even below $1\ \text{nm}$ under carefully controlled stress and interface conditions, breaking the traditional size limitation of perovskite ferroelectrics (Banerjee *et al.*, 2022). Factors contributing to this include a short coherence length, strong ionic bonding, and interfacial electric fields that support domain nucleation as depicted in Table 1. The stabilization of the orthorhombic $Pca2_1$ phase at nanoscale thickness is governed by coherence length, interface strain, and oxygen-vacancy-driven dipole ordering.

The wake-up effect, which can be caused by the increase in remanent polarization after initial cycling observed across all thicknesses but is more pronounced in ultrathin films. This arises from the higher interfacial trap density and partially pinned dipoles at early cycles. Cycling induces oxygen vacancy redistribution and alignment of defect-dipole complexes, activating previously inactive domains and resulting in stronger polarization switching. Therefore, thickness not only defines the ferroelectric phase stability but also strongly affects wake-up kinetics, endurance, and retention. Optimizing dopant concentration, annealing profile, and electrode stress for each regime is crucial to ensure reproducible ferroelectricity down to the atomic scale.

Table 1. Thickness dependent Ferroelectric behaviour of HfO₂

Thickness Regime	Typical Materials / Dopants	Key Processing Conditions	Ferroelectric Behavior
< 1 nm (ultrathin tunnel barriers)	Hf _{0.5} Zr _{0.5} O ₂ , Si:HfO ₂	High-stress electrodes (W, TiN), rapid annealing (350-450°C)	Confirmed switchable polarization; tunneling electroresistance dominant (Jiang <i>et al.</i> , 2021; Liao <i>et al.</i> , 2023).
2–5 nm (high-scalability memory window)	Zr, Si, Al, Y (3-10 at.%)	RTA 400-600°C, oxygen - controlled interfaces	High Pr (10–30 $\mu\text{C cm}^{-2}$), stable wake-up behavior (Luo <i>et al.</i> , 2021; Song <i>et al.</i> , 2021b).
> 5–10 nm (enhanced polarization regime)	La, Gd, Y	Moderate stress annealing 500-700 °C	High polarization but risk of monoclinic relaxation and leakage increase (Hsain <i>et al.</i> , 2022).

Table 2. Dopant and Annealing effect on HfO₂

Dopant System	Film Thickness (nm)	Optimal Annealing Temperature (°C)	Ferroelectric Stabilization
Zr (Hf _{1-x} Zr _x O ₂)	2-10	350-500	Stabilizes orthorhombic phase via lattice strain and oxygen vacancy control; preferred for sub-10 nm nodes (Mimura <i>et al.</i> , 2021).
Si-HfO ₂	3-8	450-600	Suppresses monoclinic relaxation and enhances remanent polarization through Si-O bonding (Alrifai, 2024).
Y / Gd-HfO ₂	8-20	500-700	Promotes larger grains and higher Pr, but excessive oxygen deficiency may increase leakage (Cheng <i>et al.</i> , 2025).
La-HfO ₂	10-30	550-750	Facilitates large-volume orthorhombic regions; high temperature required for complete crystallization (Juyoung Jeong <i>et al.</i> , 2024).
Al-HfO ₂	2-10	400-550	Improves endurance; fine grains help maintain phase stability during cycling (Jiae Jeong <i>et al.</i> , 2024).

Table 3. Annealing effect on HfO₂ deposited using ALD and Sputtering

Growth Method	Initial Film Structure	Effect of Annealing	Impact on Ferroelectricity
ALD	Amorphous, uniform, atomically smooth interfaces	Stress-induced phase transformation favored at lower temperatures (400-500 °C)	Enhanced orthorhombic stabilization under reduced thermal budget; suitable for CMOS integration (Kim <i>et al.</i> , 2023).
Sputtering	Columnar grains, higher residual stress	Requires precise ramp-rate control to avoid excessive grain coarsening	Over-annealing can induce monoclinic reversion; careful oxygen control essential (Jaszewski <i>et al.</i> , 2022).

Effect of Annealing and Crystallization

Post-deposition annealing (PDA) is a decisive factor governing the formation and stability of the ferroelectric orthorhombic $Pca2_1$ phase in doped HfO₂ thin films. The annealing temperature, time, and ramp rate determine oxygen vacancy migration, grain nucleation, and stress relaxation, which in turn influence the coexistence of orthorhombic, tetragonal, and monoclinic phases. Grain size, phase purity, and texture control during annealing are vital to maximize polarization and reduce leakage (Narasimhan *et al.*, 2021). Different dopants alter the energy landscape of phase stabilization and thus require specific annealing conditions. Table 2 summarizes the typical dopant concentrations, film thickness regimes, and optimal annealing ranges.

The Influence of annealing temperature on the HfO₂ thin film deposited using ALD and sputtering

has been illustrated in Table 3. The film's initial microstructure significantly affects its response to thermal processing. In ALD-grown films, interfacial stress and dopant distribution during RTA promote the formation of the ferroelectric orthorhombic phase at relatively low thermal budgets. In contrast, sputtered films, due to higher defect density and local compositional variations, often require optimized oxygen partial pressure and slower heating ramps to achieve similar phase purity.

The presence of a capping layer strongly influences the ferroelectric phase evolution during annealing. A metal cap exerts biaxial compressive stress and alters interfacial oxygen activity, both of which help stabilize the $Pca2_1$ phase.

- **TiN Cap:** Provides the most effective phase stabilization due to thermal expansion mismatch and nitrogen scavenging. TiN/HfO₂

- stacks typically yield high remanent polarization ($10\text{--}30 \mu\text{C cm}^{-2}$) and reduced wake-up.
- **W and Ru Caps:** Offer moderate stress but higher thermal conductivity, leading to faster grain growth and slightly increased leakage.
 - **Uncapped Films:** Tend to relax into the monoclinic non-ferroelectric phase due to lack of confinement stress; reduced polarization and endurance are typically observed.

Additionally, symmetric capping (metal-ferroelectric-metal) can mitigate asymmetric stress gradients, improving switching endurance and reducing imprint effects.

Domain Structure and Scaling Implications

Ferroelectric HfO_2 films are polycrystalline, with domains spanning a few to tens of nanometers. Domain wall motion is strongly affected by grain boundaries, interfaces, and local defects. At sub-10 nm scales, domain pinning, nucleation variability, and clamping effects dominate, impacting device uniformity and fatigue. Designing FeFETs appropriate for massively scaled nodes requires an understanding of these nanoscale domain phenomena.

Materials and Process Engineering

The ferroelectric layer's manufacturing parameters and material quality have a significant impact on the performance and dependability of HfO_2 -based FeFETs. Deposition methods, thermal treatment, and electrode engineering all affect crucial factors as phase stability, doping, grain structure, and interface integrity. The main techniques for optimizing ferroelectric HfO_2 films for sophisticated device integration are described in this section.

Deposition Techniques for Ferroelectric HfO_2

The industry standard technique for HfO_2 -based films is Atomic ALD because of its atomic-scale thickness control, homogeneity, and compatibility with CMOS nodes (Wei *et al.*, 2024). ALD produces dense, conformal films by alternating cycles of Hf precursors (e.g., HfCl_4 , TDMA-Hf) and oxidants (H_2O , O_3). Supercycle arrangements are used to create doped versions such as $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$ (HZO). Post-deposition annealing (PDA) is necessary for the amorphous as-deposited films to crystallize into the ferroelectric orthorhombic phase. Although less popular, sputtering provides greater flexibility and throughput. Using Hf-Zr alloy targets in Ar/O_2

environments, sputtered HZO films can achieve ferroelectric properties with optimized oxygen flow and annealing. Though phase coexistence (orthorhombic and monoclinic) is common, sputtering allows better control over grain size and oxygen content as evident from Figure 2a and Figure 2b. The phase distribution of HfO_2 can be optimized by doping Si, Al, Y, and Zr.

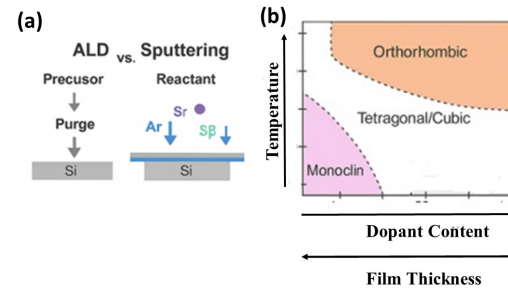


Figure 2. Material engineering of HfO_2 -based FeFETs. (a) ALD vs. sputtering process comparison, (b) window map showing phase evolution with temperature, thickness and dopant

Interface and Electrode Effects

The choice of electrode significantly affects polarization behavior, leakage, and retention. Materials like TiN, W, Ru, and IrO_2 are favored for their thermal stability and work function alignment (Chen *et al.*, 2022). Asymmetric electrode stacks (e.g., TiN/HZO/W) may introduce built-in electric fields, causing hysteresis shifts (imprint), while symmetric configurations can reduce such effects. Interfacial oxides at the silicon interface can create fixed charges and traps, degrading data retention and uniformity (Pešić *et al.*, 2018).

Interface and Electrode Engineering

Electrode Material Selection and Its Impact

In HfO_2 -based FeFETs, electrode material selection plays a pivotal role in determining ferroelectric phase stability, interface behavior, and overall device reliability (Koo *et al.*, 2025). Common electrode materials include TiN, W, Pt, Ru, and conductive oxides such as RuO_2 and IrO_2 . Titanium nitride (TiN) is widely favored for its compatibility with CMOS processes and its ability to provide mechanical confinement during post-deposition annealing (Mahajan *et al.*, 2024). However, TiN can chemically react at the interface to form substoichiometric TiO_xN_y , contributing to oxygen vacancy formation within the ferroelectric

layer. While moderate oxygen vacancies can stabilize the orthorhombic phase, excess vacancies lead to increased leakage, retention loss, and fatigue (Zhao *et al.*, 2024). Tungsten (W) electrodes introduce tensile stress during annealing, which favors the formation of the orthorhombic ferroelectric phase. W also exhibits lower reactivity with HfO_2 , resulting in improved endurance and stability (Lee *et al.*, 2025). Noble metals like Pt and Ru are chemically stable and resist oxidation, but they can introduce thermal mismatch and grain coarsening effects, which may disrupt film uniformity. Conductive oxides like RuO_2 offer excellent oxygen barrier properties but must be carefully optimized, as their strong oxidative behavior may destabilize the ferroelectric phase (Kwon *et al.*, 2010).

Interfacial Chemistry and Oxygen Vacancy Formation

At the nanoscale, interface chemistry becomes a dominant factor influencing ferroelectric switching. During deposition and subsequent annealing, reactions between HfO_2 and the electrode or substrate can lead to the growth of interfacial oxides, such as native SiO_2 or suboxides from the electrodes (Banerjee *et al.*, 2022). These layers can inhibit domain switching, introduce fixed charges, and lead to polarization fatigue.

Elemental diffusion, especially of Ti from TiN or oxygen from the ambient, alters the vacancy profile within the HfO_2 layer. Since oxygen vacancies are essential for stabilizing the orthorhombic phase but also increase trap density and leakage current, their concentration must be carefully managed (Materano *et al.*, 2021). Techniques like in-situ stack deposition, the use of barrier layers (e.g., Al_2O_3 , TiAlN), and low-pressure annealing have proven effective in minimizing interfacial degradation and ensuring controlled oxygen vacancy profiles.

Mechanical Stress and Phase Stability

Mechanical stress exerted by the electrode materials during thermal treatment significantly influences the stabilization of the orthorhombic phase. Tensile stress, commonly introduced by W or Ru electrodes, enhances orthorhombic phase formation, whereas compressive stress depending on its magnitude and direction can either support or suppress it. The mechanical confinement also affects the orientation of grains and polarization vectors, which are critical for achieving strong remanent polarization and minimizing wake-up effects as evident from Figure 3a and Figure 3b (Mo *et al.*, 2025). Finite element modeling and X-ray diffraction studies have demonstrated that slight

variations in electrode thickness, material composition, or annealing profiles can cause measurable changes in stress distribution, thus impacting ferroelectric yield and uniformity as depicted from Figure 3c and Figure 3d (Fernandez *et al.*, 2022).

Electrical Effects at Interfaces: Depolarization and Imprint

Electrical phenomena such as depolarization fields and imprint are governed by the electrode-ferroelectric interface (Liu *et al.*, 2016). Incomplete charge screening at the interface leads to depolarization fields that counteract spontaneous polarization, especially in ultrathin films. These fields can cause back-switching of domains, compromising data retention and stability. Moreover, asymmetric electrodes or uneven trap distributions can induce built-in electric fields, resulting in imprint manifested as shifts in the polarization hysteresis loop (Chen *et al.*, 2025). This imprint effect degrades performance in memory applications by narrowing the memory window and introducing read errors. Solutions include symmetric electrode stacks, optimized work function alignment, and dipole engineering at the interface. In FeFETs, the interface between ferroelectric HfO_2 and the underlying semiconductor channel (e.g., silicon or SiGe) directly affects threshold voltage modulation and the overall memory window. The presence of a native or deposited SiO_2 layer can screen the polarization field, reducing the efficiency of charge modulation and increasing the density of interface traps (D_{it}). These traps capture and release carriers during operation, resulting in endurance degradation and device variability. To address this, high- κ interlayers such as La_2O_3 or Al_2O_3 are introduced to reduce D_{it} and enhance electrostatic coupling. Advanced surface cleaning methods and direct epitaxial growth techniques are also employed to achieve abrupt, defect-free interfaces. Several advanced techniques are employed to optimize ferroelectric interfaces. These include pre-cleaning to remove native oxides, in-situ deposition to prevent contamination, and buffer layers to control oxygen exchange. Thermal budgets are minimized using low-temperature rapid thermal annealing (RTA) or multi-step anneals to suppress interfacial diffusion. Emerging methods such as atomic layer etching (ALE), plasma surface treatments, and molecular passivation with self-assembled monolayers (SAMs) offer atomic-level control over surface chemistry and trap density. Implementing these strategies enhances endurance, suppresses wake-up effects, and improves the stability and reproducibility of FeFETs.

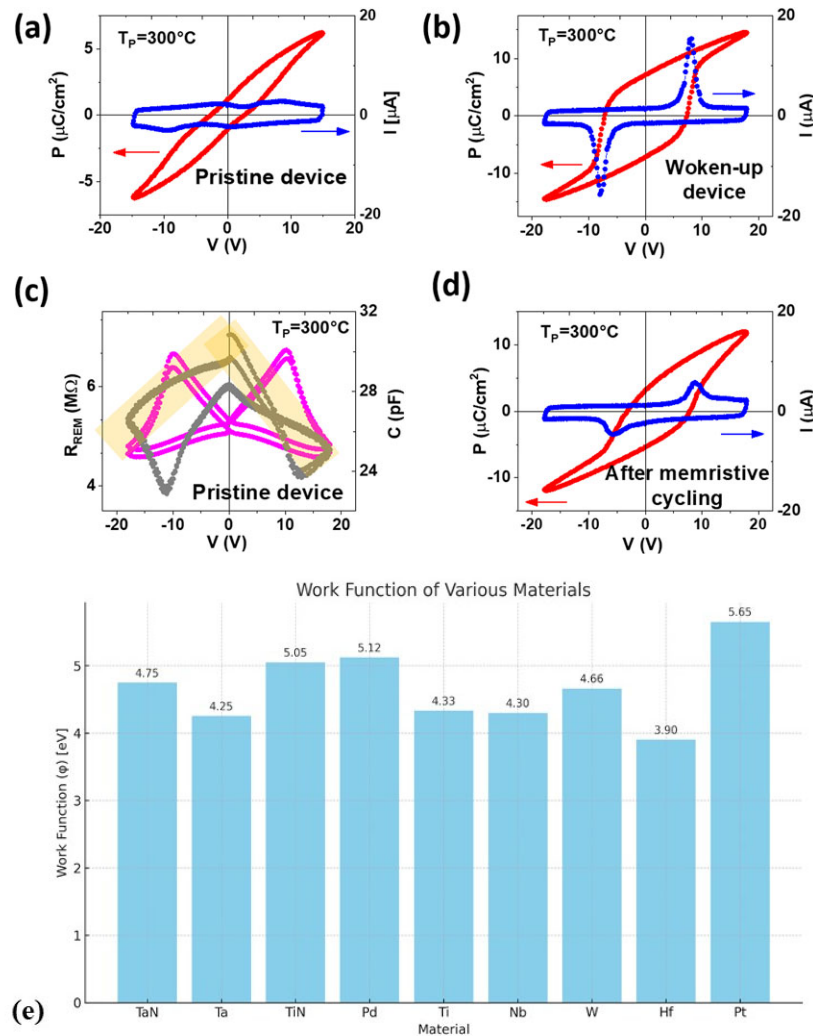


Figure 3. Electrical characteristics of Pt/Ca:HfO₂ devices. (a-b) I-V (blue) and P-V (red) curves before and after wake-up (10³ cycles), showing ferroelectricity development. (c-d) C-V (magenta) and R-V (gray) curves at 100 kHz; subsequent I-V and P-V confirm ferroelectricity. © Ferreyra *et al.* (Ferreyra *et al.*, 2025), 2025, CC BY 0. (e) Work functions of different electrodes

FeFET Device Architectures

The advancement of FeFET device architectures is crucial to fulfilling the requirements of future non-volatile memory (NVM) and logic-in-memory applications (Yin *et al.*, 2018). As semiconductor scaling approaches sub-10 nm nodes, integrating ferroelectric HfO₂ into various transistor structures enables better performance, reduced area, and CMOS process compatibility. Key FeFET architectures include planar, 3D, and nanoscale configurations, each with unique benefits and challenges as shown in Figure 4.

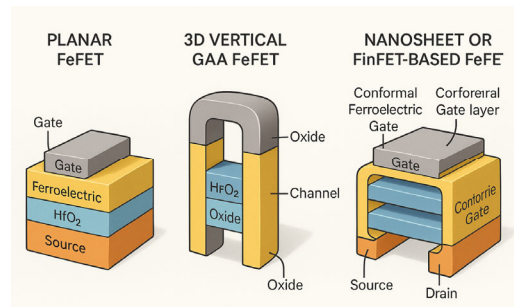


Figure 4. FeFET Architectures

Planar FeFETs

Planar FeFETs are the simplest and most established form, using a ferroelectric HfO_2 layer (commonly doped with Zr or Si) inserted between a metal gate (e.g., TiN, W) and a semiconductor channel (typically Si or SiGe). These devices operate via polarization-induced threshold voltage shifts that modulate channel conductivity. Their metal - ferroelectric - semiconductor (MFS) or metal - ferroelectric - insulator - semiconductor (MFIS) stack can be fabricated using standard gate - first or gate-last flows, ensuring strong compatibility with existing CMOS platforms. Planar FeFETs offer low - power operation, fast switching, and non-volatility, making them viable DRAM alternatives. However, their scalability below the 22 nm node is limited. As dimensions shrink, challenges such as leakage, wake-up effects, and variability increase. Maintaining endurance over 10^{10} cycles and retention beyond 10 years is also demanding from a materials integration standpoint.

3D FeFETs

To overcome planar limitations and enhance density, 3D FeFET architectures utilize vertical channels formed in deep trenches or pillars, with ferroelectric gates wrapped around the channel. This allows multi-layer memory stacking without expanding the footprint, similar to 3D NAND. Vertical FeFETs rely on ALD for conformal gate stack formation and uniform polarization control. Superior electrostatic control and short-channel suppression are made possible by the ferroelectric gate completely enclosing the channel in gate-all-around (GAA) FeFETs, a 3D variation that is crucial for nodes smaller than 10 nm. Despite its potential, 3D FeFETs have difficulties controlling interfacial quality, preserving thermal stability during back-end integration, and establishing uniform phase formation in high aspect-ratio structures.

Nanosheet and FinFET FeFETs

Ferroelectric layer integration into these cutting-edge platforms is crucial for the broad adoption of FeFETs as the industry shifts to FinFET and nanosheet transistors. The gate of FinFET-based FeFETs encircles a silicon fin, improving short-channel immunity and gate control. The gate metal is formed after the ferroelectric HfO_2 layer is conformally layered over the fin. This is extended by nanosheet FeFETs, which provide even more electrostatic control and reduced variability by using horizontally stacked sheets or nanowires in

a complete GAA arrangement. Applications requiring compute-in-memory and high-density memory are ideally suited for these structures. Low-temperature procedures, superior interface passivation, and ultra-thin film management are necessary for incorporating ferroelectric materials into these nanoscale structures. Reducing interfacial oxides, controlling mechanical stress, and refining defect profiles are important engineering problems that guarantee stable and consistent polarization behavior.

Reliability and Scaling Challenges

Overcoming reliability and scale issues is essential to the commercialization of HfO_2 -based ferroelectric field-effect transistors (FeFETs). FeFETs have appealing advantages including fast switching, low power consumption, and CMOS compatibility, but with time, endurance limitations, retention loss, device variability, and size-related restrictions can cause their performance to deteriorate as shown in Figure 5.

Endurance Retention and Imprint

The ability of a FeFET to tolerate frequent switching is known as endurance, and it is a crucial consideration. FeFETs typically demonstrate 10^7 - 10^9 cycles, although optimized structures can exceed 10^{11} cycles. Degradation occurs due to defect accumulation, especially oxygen vacancies and interfacial charge traps, along with phase transitions to non-switchable monoclinic forms. Initially, devices exhibit a ‘wake-up’ effect, where polarization improves with cycling but later show fatigue and reduced remanent polarization. Strategies such as optimizing annealing, doping profiles, and introducing buffer or passivation layers help mitigate fatigue and extend endurance. Retention refers to the ability to maintain the polarization state over time without power. In thin ferroelectric films, retention is compromised by depolarization fields, interfacial charges, and non-uniform electric fields. Additionally, incomplete charge screening at the electrodes can cause polarization back-switching. Imprint, another issue, shifts the hysteresis loop due to built-in fields from asymmetric electrodes or trapped charges, leading to a favored polarization state and reduced data reliability. Symmetric gate stacks and optimized annealing reduce both imprint and retention degradation.

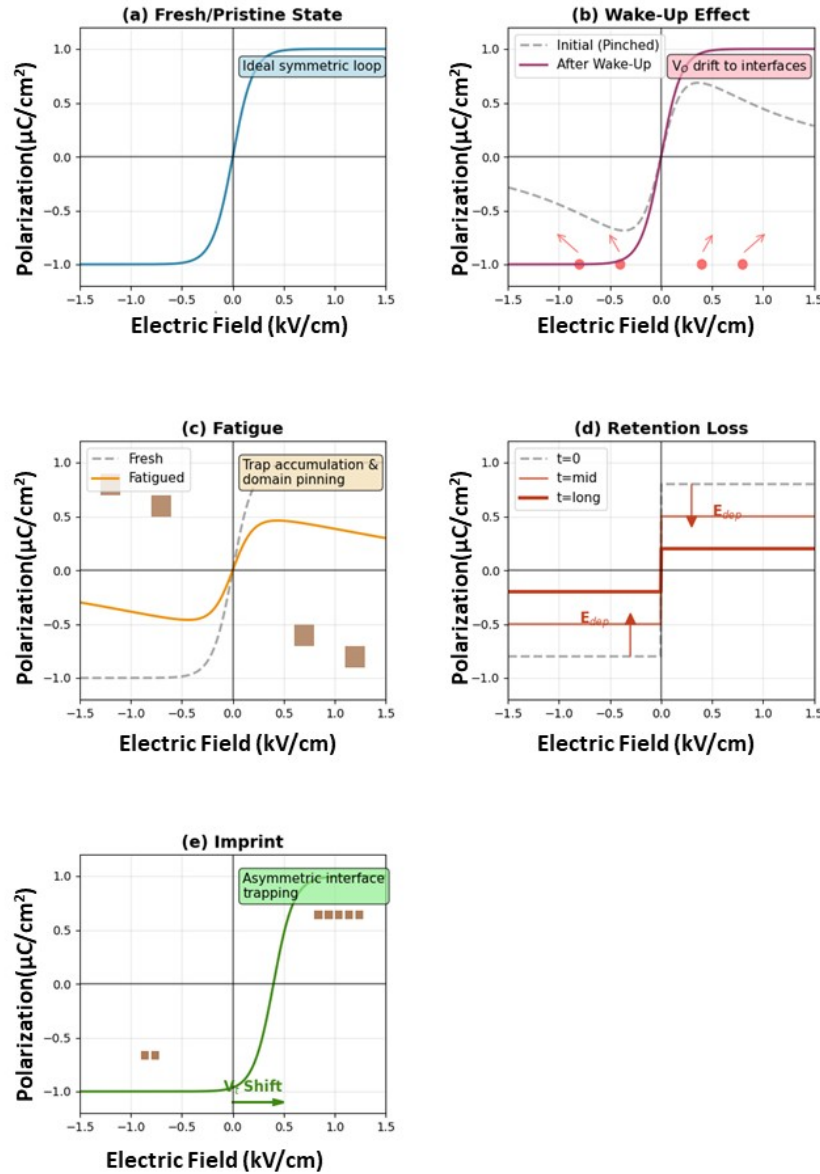


Figure 5. Major reliability based mechanisms in HfO_2 based FETs (a) Pristine state, (b) Wake up effect, (c) Fatigue, (d) Retention loss, and (e) Imprint

Wake-Up and Fatigue

The wake-up effect which can be observed as an initial improvement in polarization is typically caused by the redistribution of oxygen vacancies and activation of initially inactive regions. However, with extended cycling, fatigue sets in due to domain wall pinning, interfacial degradation, and transition to non-ferroelectric phases. Using stable electrodes, refined doping strategies, and optimized thermal processing helps enhance long-term polarization retention and reduce fatigue.

Sub-10 nm Scaling and High Temperature Stability

As FeFETs scale to sub-10 nm nodes, maintaining ferroelectricity becomes increasingly difficult. Ultrathin films (3-5 nm) experience stronger depolarization, increased interfacial effects, and reduced grain size. Integrating ferroelectric layers into FinFETs and nanosheets requires uniform, conformal deposition and high orthorhombic phase purity. Moreover, shrinking process thermal budgets challenge the high-

temperature annealing needed for phase stabilization. Alternatives such as laser and microwave annealing, as well as defect engineering, are under investigation. For industrial and automotive environments, FeFETs must remain stable under wide temperature and humidity ranges. High temperatures can increase leakage, activate traps, and destabilize the ferroelectric phase, while environmental exposure may cause moisture ingress and chemical degradation. To guarantee dependability in practical settings, solutions include moisture-resistant packing, thermal barrier coatings, and sturdy encapsulation.

Applications and Future Outlook

Ferroelectric field-effect transistors (FeFETs) based on hafnium oxide (HfO_2) are quickly becoming a multipurpose technology that connects logic, memory, and neuromorphic computing. They are a top contender for next-generation electronic systems because of their non-volatility, low power consumption, quick switching, and complete CMOS compatibility. The main application areas and the prospects for broad FeFET adoption are highlighted in this section.

Embedded Non-Volatile Memory (eNVM) For Compute in memory and Neuromorphic Computing

FeFETs are highly suitable for embedded non-volatile memory in SoCs, microcontrollers, and IoT devices. FeFETs provide superior scalability below 10 nm, faster write speeds (<10 ns), and a lower programming voltage (<3 V) than conventional flash or EEPROM. They are inexpensive and simple to integrate with conventional CMOS processes because of their straightforward 1T cell structure, which does away with the need for intricate selection devices.

By carrying out computation directly within memory arrays, FeFETs make it possible for compute-in-memory (CIM) architectures to overcome the von Neumann bottleneck. They are appropriate for in-memory vector-matrix multiplications, which are essential for AI inference, due to their quick switching and analog polarization states. FeFETs are perfect for edge AI systems that need effective real-time processing because they can also operate in a hybrid digital-analog mode. Because FeFETs can replicate synaptic behavior, they are being investigated for neuromorphic computing. Their multi-level and progressive switching facilitates learning mechanisms such as spike-timing dependent plasticity (STDP) by simulating biological

synapses. FeFETs are perfect for energy-efficient neural network accelerators because of their great endurance and low energy consumption.

Hardware Security and Edge Electronics

FeFETs' non-linear switching and intrinsic process changes enable the development of physically unclonable functions (PUFs) for secure key generation. FeFET-based memory arrays can also support in-memory encryption and secure data paths, opening avenues for tamper-resistant, hardware-rooted security solutions, particularly in edge and IoT devices.

FeFETs' low power usage, fast speed, and small area make them ideal for portable and wearable electronics. Their non-volatility ensures data retention during power-off states, crucial for battery-powered and intermittently powered systems. Their potential for flexible substrate integration further supports wearable applications.

Conclusion

HfO_2 -based FeFETs offer a powerful solution for next-generation non-volatile memory and logic devices due to their intrinsic ferroelectricity, CMOS compatibility, and scalability to sub-10 nm nodes summarized in Table 4. Their low power consumption, fast switching, and analog programmability make them ideal for applications in embedded memory, AI acceleration, and neuromorphic computing. While challenges like endurance, retention, and variability remain, ongoing advancements in materials engineering and device architecture continue to improve performance. As the demand for energy-efficient and intelligent electronics grows, FeFETs are positioned to become a key enabler of future computing platforms across memory, logic, and secure hardware domains.

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Author Contributions

Conceptualization: R.K.J.; Methodology: R.K.J.; Investigation: R.K.J.; Data Curation: R.K.J.; Writing - Original Draft: R.K.J.; Writing - Review & Editing: R.K.J.; Supervision: R.K.J. All authors have read and agreed to the published version of the manuscript.

Table 4. Reports on HfO₂-based ferroelectric capacitors

Reference	Structure	Deposition Method	HfO ₂ Thickness (nm)	Deposition/Annealing Temperature (°C)	Remnant Polarization 2Pr (μC cm ⁻²)	Coercive field 2Ec (MV cm ⁻¹)	Endurance
(Siannas <i>et al.</i> , 2022)	TiN/ Hf _{0.5} Zr _{0.5} O ₂ /Ge	PAMBD	5 nm	100/-	-	-	-
(Yadav <i>et al.</i> , 2021)	TiN/ Hf _{0.5} Zr _{0.5} O ₂ /NSTO	ALD	2.2	250/550	20	2	NA
(Jiang <i>et al.</i> , 2022)	W/ Hf _{0.5} Zr _{0.5} O ₂ /IrOx	ALD	4.53	300/400	10	2	10 ⁶
(Cheema <i>et al.</i> , 2022)	TiN/W/HZH trilayer/SiO ₂ /Si	ALD	2	270/250	7.65	5.3	-
(Xu <i>et al.</i> , 2022)	La:HfO ₂ /LSMO/STO	PLD	4	600/-	-	-	-
(Prasad <i>et al.</i> , 2021)	Hf _{0.5} Zr _{0.5} O ₂ /LSMO/STO	PLD	1	700/-	-	-	-
(Liang <i>et al.</i> , 2021)	TiN/ Hf _{0.5} Zr _{0.5} O ₂ /TiN	ALD	5	250/600	41	2.4	10 ¹⁰
(Gao <i>et al.</i> , 2021)	Pt/ Hf _{0.5} Zr _{0.5} O ₂ /NSTO	ALD	1.5	250/700	4	2	-
(Song <i>et al.</i> , 2021a)	Pt/La:HfO ₂ /LSMO/Si	PLD	4.5	700/-	51	8	10 ¹⁰
(Chu <i>et al.</i> , 2021)	Ni/Al ₂ O ₃ / Hf _{0.5} Zr _{0.5} O ₂ /TiN	ALD	5	-700	10	6	10 ⁷
(Oh <i>et al.</i> , 2020)	W/ Hf _{0.5} Zr _{0.5} O ₂ /Pt	ALD	2.5	250/400	18	2.9	-
(Goh <i>et al.</i> , 2020)	TiN/ Hf _{0.5} Zr _{0.5} O ₂ /W	ALD	4.5	-600	26	3	-
(Chen <i>et al.</i> , 2019a)	TaN/Hf _{0.5} Zr _{0.5} O ₂ /SiO ₂ /Si	ALD	5	-600	-	-	10 ⁶
(Li <i>et al.</i> , 2019)	Cr/Au/Si:HfO ₂ /NSTO	PLD	4.8	700/-	51	9	-
(Chen <i>et al.</i> , 2019b)	Mo/ Hf _{0.5} Zr _{0.5} O ₂ /TiN	ALD	5	-500	58	3.2	10 ⁵
(Walters <i>et al.</i> , 2018)	TiN/ Hf _{0.5} Zr _{0.5} O ₂ /Ge	ALD	4.8	175/500	25.2	2.5	10 ¹⁰
(Tian <i>et al.</i> , 2018)	Au/ Y:HfO ₂ /Ge	RF-Sputtering	3	RT/650	3.5	3.3	-
(Chouprik <i>et al.</i> , 2017)	TiN/ Hf _{0.5} Zr _{0.5} O ₂ /Si	ALD	2.5	240/400	1	24	-
(Jha <i>et al.</i> , 2020)	TiN/HfO ₂ /TiN	ALD	10	200/500	8	2.5	10 ¹²
(Jha <i>et al.</i> , 2025)	TiN/HfO ₂ /TiN	RF-Sputtering	10	RT/500	2.4	0.5	10 ¹²

Ethics Statement

Ethical approval was not required for this study because it did not involve human participants, animals, identifiable personal data, or materials requiring institutional ethical review.

Declaration of Generative AI Use

During the preparation of this manuscript, the authors used Open AI to assist with some figures. All AI-assisted outputs were critically reviewed, verified, and revised by the authors, who accept full responsibility for the content of this manuscript.

Conflict of Interest

The authors declare that they have no conflicts of interest related to this work

Data Availability Statement

No new data were generated or analyzed in support of this research.

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