

DESIGN OF AREA & POWER EFFICIENT MGDI FULL ADDER USING POWER GATING TECHNIQUE

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Received: April 20, 2023; Revised: May 24, 2024; Accepted: June 06, 2024

Abstract

Full adders are used in many low-power circuits, digital signal processors, microprocessors, and microcontrollers, which are essential components for many digital systems. This article proposed an area and power-efficient power-gated Modified Gate Diffusion Input (MGDI) full adder architecture. An MGDI approach enhances the threshold voltage drop and overcomes weak voltage swing output. In IC design, power gating is employed to reduce power consumption by turning off the current to these opened circuit lumps. The power-gated MGDI full-adder occupies less power and has better performance as compared to conventional adders. The proposed power-gated- MGDI full-adder was constructed using Cadence Virtuoso using 45 nm technology. The results of the simulation indicate a 21.2% power consumption and a 46.4% delay reduction. The performance of the power-gated MGDI full-adder for practical applications has been assessed by designing a 32-bit carry propagation adder structure by cascading the suggested 1-bit full adder design. The proposed 32-bit carry propagation adder occupies less delay and power.

Keywords: CMOS; Full adder; Gate diffusion input; Modified gate diffusion input; Power gating

Introduction

Nowadays, the design complexities in ICs are increasing exponentially. There is an urge to develop and examine such power-reducing techniques, which could provide low power consumption, less complex design, high-speed performance and high reliability without compromising any functionality of a circuit design. Currently, the most popular technology used to design circuits is CMOS technology, but

it dissipates significant power during transistor switching activity and leakage current flow. The systematic designs have demanded mathematical calculations at minimal power and fast speed. Full adders are recognizable as a hallmark of excellent performance and low power. Full adder plays a significant role in low-power architectures (Rabaey *et al.*, 2003).

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A full adder is predominant in high-speed data communication architecture in VLSI. The Full adder circuits are used in network switches, digital signal processors and low-power circuits. These characteristics contrasted with typical power, delay and speed. The current full adder circuit's main goal is to minimize power dissipation and area. The MGDI full adder, Gate Diffusion Input (GDI) full adder, and the power-gated MGDI full adder are evaluated.

Motivation

Adders are widely used in VLSI systems like DSP processors, and microprocessors. Adders are often located along an essential step in digital systems, which affects the system's overall performance. Therefore, improving the adder's performance is increasingly becoming a priority. In adder designs, the power gating method is utilized to reduce power consumption. The key aspects and benefits of using power-gated MGDI full-adder is

- The MGDI logic architecture consumes less power than CMOS logic.
- Power is turned off whenever the circuit is lumped in the GDI full adder circuit, which uses power gating technology to reduce the circuit power dissipation.
- Reducing stand-by or leaking power using IDDQ testing is the primary benefit of power gating.
- Compared to a traditional adder, a power-gated MGDI
- full-adder performs better and consumes less power.

The objective of the proposed power-gated MGDI full adder is

- a. It occupies less power than conventional Full adder architectures.
- b. It performs the circuit operation with less delay and utilizes only 8 transistors.

Prior Work

This article aims to use the GDI approach for a full adder with better performance. Compared to all existing designs, this proposed design will be faster and have a higher system efficiency. The design can be further altered by including a few extra transistors. Navi *et al.* (2009) proposed a high-performance low-power full adder cell using static CMOS inverter circuits. The successful implementation of a low-power 8T GDI complete full-adder architecture using the variable body biasing technique is implemented using 90 nm

CMOS Technology (Solomon *et al.*, 2018). The low power techniques used in the IC design, the VBB approach effectively reduces static power usage. An analysis of comparing the full adder circuit designs in classic bias mode and VBB method mode regarding power consumption and the proportional delay are discussed. Tanner EDA and TSMC MOSIS, a t25 nm technology, were acclimated to verify and differentiate the performance of this MGDI with traditional GDI and CMOS logic regarding transistor count, delay, and delay power dissipation (Zimmermann and Fichtner, 1997). Pass transistor logic (PTL) has lower output swings and a lower threshold voltage drop than a single-channel transistor, it performs poorly in terms of power consumption when compared to CMOS, GDI and MGDI. Globally, numerous research institutions focus on low-power IC for many uses (Dhanasekar, 2023). Altogether, this survey reveals that compared to current GDI, CMOS, and PTL, the updated simple and other full adders have the minimum delay, the lowest power consumption, and occupy only a few transistors (Tejaswini *et al.*, 2020). Lee *et al.* (2007) suggested a unique 10-transistor full adder implemented using a GDI structure (Lee *et al.*, 2007). Full adder cells have been made by employing a different internal logic structure. Two full adders are constructed in conjunction as PTL powerless or groundless types of logic to illustrate its benefits. They were developed using TSMC's 0.18 m CMOS, tested in simulations and contrasted with other recently announced energy-efficient full adders.

A Transmission Gate Full Adder (TGA) circuit uses 16 transistors to reduce the power consumption in digital architectures. The Transmission Function Full Adder (TFA), which makes use of 20 transistors, was proposed by Shams *et al.* (2002). Transmission gates and transmission function theory provide the basis for these adders. Although low power consumption is the primary advantage of transmission gate logic structures, their weak driving capabilities make them less desirable for cascading TGAs or TFAs in complicated structure design. Digitalization will impact most engineering fields, with fast data transmission networks and wide-area communication networks with the most significant impact (Dhanasekar *et al.*, 2019; Govindaraj *et al.*, 2024). The most effective strategy for adders provided in this study, in-between buffer insertion used during the modelling of the circuit topology is discussed in an analysis to increase the power of adder cells (Babu *et al.*, 2021). A high-performance arithmetic circuit with mixed full adder topologies has attained low power has been discussed (Alioto *et al.*, 2007; Kattepogu and Tripathi, 2024).

Contribution

In this article, we investigated the implementation of full adders utilizing MGDI and GDI techniques, with a particular focus on power-gating-based MGDI full adders. Our findings demonstrate the effectiveness of these techniques in optimizing power consumption and area utilization within silicon chips. A 45 nm CMOS technology is used to implement the proposed adder design which leads to significant reductions in both power consumption (21.2%) and delay (46.4%) than the traditional adder designs. Specifically, it consumed 1.851 pW of power, achieved a delay of 0.173 μ s, and utilized only 8 transistors. The incorporation of the MGDI method played a pivotal role in enhancing the threshold voltage drop while preventing voltage swings in the output, thus contributing to the overall efficiency of the design. By employing power-gating techniques, we effectively minimized power consumption by intelligently switching off the current when not in use.

The Modified Gate Diffusion Input, Gate Diffusion Input, and power-gated MGDI for Inverter design are discussed in section 2. In Section 3, MGDI and GDI for full adder were methodically explained. The modified gate diffusion full adder with the Power Gating technique was proposed in section 4. Section 5 provides the result analysis of the power-gated MGDI full adder design with comparison. A conclusion to the proposed design is inclined in Section 6.

GDI, MGDI and Power Gated MOD GDI Architectures

Gate Diffusion Input

A process of designing low-power digital combinational circuits, especially in a logic design, called GDI. Digital circuit size, propagation delay, and power utilization will be minimized while prolonging a low-level logic design complexity in the GDI method. The GDI cell has many benefits but its performance degrades. Furthermore, physical installation for main GDI cells is not possible with conventional p-well advancement.

Furthermore, due to distinct wells for each transistor, the primary GDI cell would have a larger area. This fundamental structure is still being determined since the source and drain modules rely on input values. In the present era, gate diffusion input is the single most popular technique. Two transistors are used in the GDI method to create logic gates. Figure 1 depicts GDI cell development. Although the GDI formation is the same as an Inverter.

It has different functionality where three inputs are carried by the GDI cell, which is mentioned below,

- G denotes as a gate input for PMOS and NMOS transistors.
- P stands for the PMOS transistor.
- N stands for the NMOS transistor.

GDI provides this ability to create logic gates using two transistors.

Modified Gate Diffusion Input

The PMOS and NMOS transistor expands in MGDI, on the other hand, remains set to GND and VDD. It handles the issues with required GDI cells and relates to the basic GDI. As a result, the GDI gates can be easily realized in standard CMOS processes. The body impact on circuit operation has a very similar outcome to a normal GDI cell.

MGDI has less power dissipation than CMOS logic architecture and GDI logic. In MGDI Transient and DC analysis is used to measure the CMOS innermost conditions related to circuit speed, total design area, circuits' power dissipation, and power delay. MGDI is the preferred logic design for realizing arbitrary combinational circuits is depicted in Figure 2.

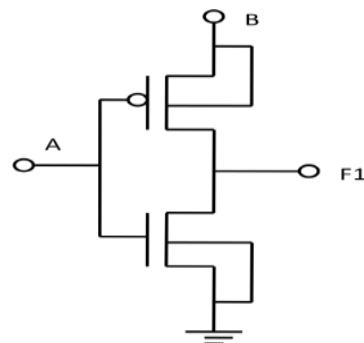


Figure 1. The basic cell of GDI

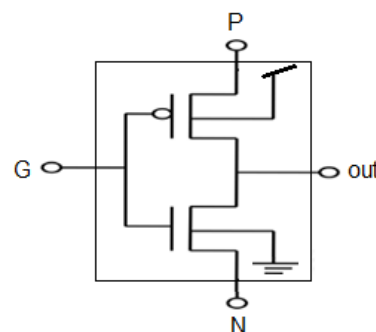


Figure 2. Basic MOD GDI Cell

Power Gated MOD GDI

By cutting off the current to the circuit, power gating is utilized in IC design to minimize power usage. Power gating can reduce stand-by or leakage power while also making IDDQ testing possible. The following parameters are used in power-gating techniques,

Power Gate Size

It should be selected in the current volume at any given time. An enormous gate is needed to ensure that the gate is not causing any discernible voltage. Typically, the switching capacitance is approximately three times the gate size. Moreover, designers have the option of using PMOS or NMOS gate. Typically, NMOS gates have a minimum surface area per unit of switching current. The switching current can be precisely measured using dynamic power analysis methods.

Gate Control Slew Rate

The high slew rate might affect the effectiveness of power gating. As a result, turning the circuit on and off takes longer. The gate control signal is buffered to adjust the slew rate.

Simultaneous Switching Capacitance

The major limitation is the maximum number of circuits that may be switched simultaneously without compromising the network's integrity. To avoid this, a circuit must be changed gradually.

Power Gate Leakage

Leakage reduction is crucial as power gates are constructed from operating transistors, allowing for the most significant possible power savings.

Figure 3 shows the fundamental power-gated MGDI. Disconnecting the path to the power and ground terminals is one straightforward approach in

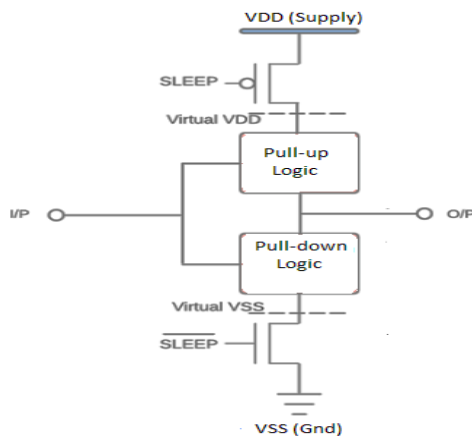


Figure 3. Basic power gating

such a circumstance. To accomplish this, a power gating circuit that can cut off the path when the circuit is dormant, i.e., not in use.

when SLEEP = OFF (0)

PMOS and NMOS sleep transistors on.

The circuit runs typically since PMOS & NMOS networks are linked to virtual VDD and GND.

when SLEEP = ON (1)

PMOS and NMOS sleep transistors turn off.

Because the direct channel from VDD to GND is cut off, leakage power is decreased.

GDI and MGDI ADDER TECHNIQUES

High Speed Adder using GDI Technique

A full adder is crucial when developing a processor. The speed of operation becomes a critical consideration as the circuit complexity rises. There are several full adder architectures are available with better performance. This article discusses the Gate Diffusion Input approach to create a low-power and high-performance full adder. GDI is a specific, modern approach to creating logical circuits (Kai *et al.*, 2019). This technique will minimize the size of digital circuits, propagation delay, and power consumption in the circuit while maintaining a minimal level of logic design complexity. This design performance is contrasted with this high-speed adder's recent full adder designs.

The GDI method is significantly more effective and has many benefits, but a few issues can be fixed. There are three inputs in a GDI cell. The CMOS Schematic diagram for Full adder using GDI-Cell is shown in Figure 4. N and P represent the input for the source and drain, the gate serves as the input for both NMOS and PMOS transistors (Amini-Valashani and Mirzakuchaki, 2020). Hence the ability to construct many functions using the GDI approach is its main advantage. Table 1 illustrates several designs, such as MUX, AND, NOT and OR gates which are used to implement GDI. The MUX design which can be accomplished using two transistors, is the most difficult of them.

Table 1. The truth table for GDI cell

N	P	G	OUT	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	$A+B$	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

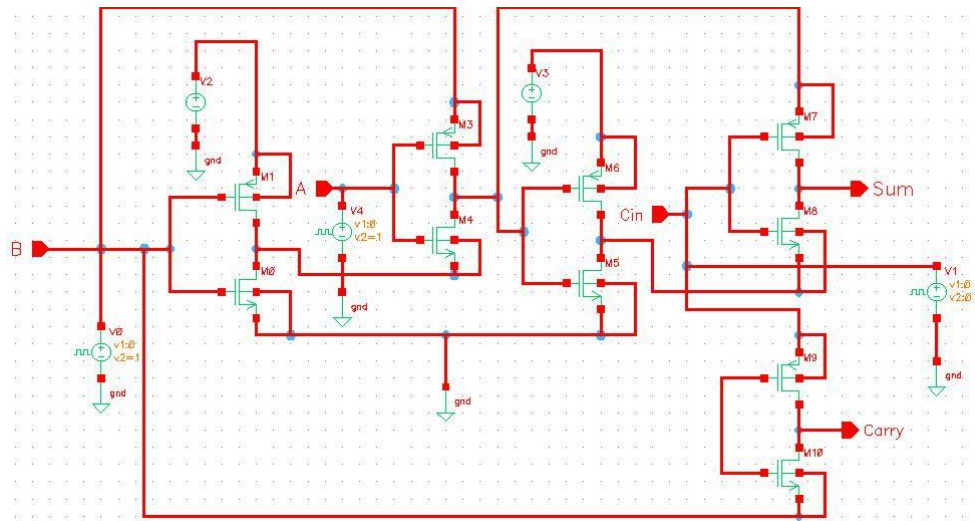


Figure 4. Full adder using GDI-Cell

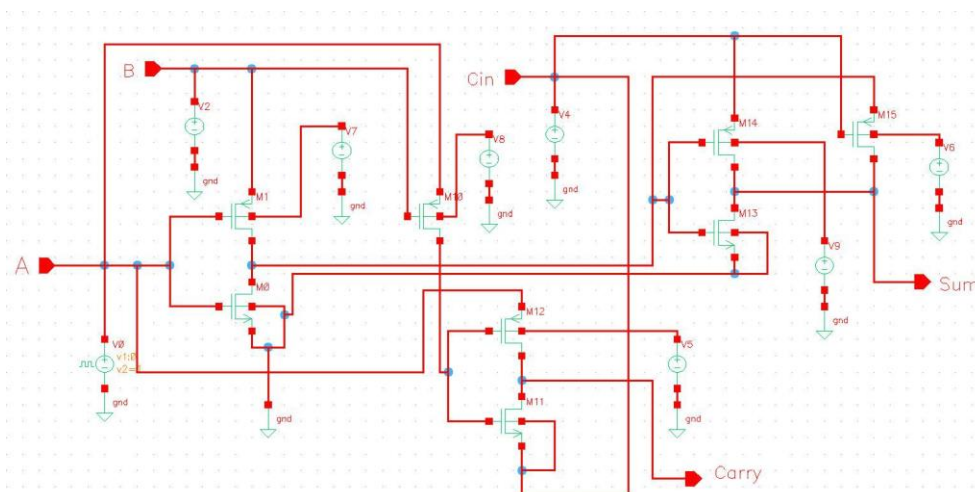


Figure 5. Full adder using MGDI-Cell

Designing a MUX takes 8-10 transistors than the traditional methods. Swing deterioration is the primary flaw of the GDI method. This is caused by threshold loss, which must be eliminated using very expensive.

Full Adder using MGDI Technique

A high-speed digital system needs additional circuits to perform specific functions. In adder cell design, the primary issues are area, power and delay in the logical circuits. The CMOS Schematic diagram for Full adder using MGDI-Cell is shown in Figure 5. Several devices must be optimized for speed and power in low-voltage and low-power applications, which is a significant problem (Aguirre-Hernandez and Linares-Aranda, 2011).

Utilizing the modified gate diffusion input technique can solve these problems. Through the use of this technology, digital circuit size, delay, and power consumption can be reduced, so logic design complexity is minimal. The performance difficulties of the existing were contrasted with GDI, CMOS logic, and MGDI techniques (Bhattacharyya *et al.*, 2015). Four terminals represent the fundamental unit of the GDI cell in PMOS and NMOS: G is the common gate input of both PMOS and NMOS, N is the NMOS outer diffusion node, P is the PMOS outer diffusion node, as well as D is the PMOS and NMOS common diffusion node (Sanapala and Sakthivel, 2019; Tyagi *et al.*, 2023). This work implements modified GDI and compares them to existing GDI and CMOS logic. A digital

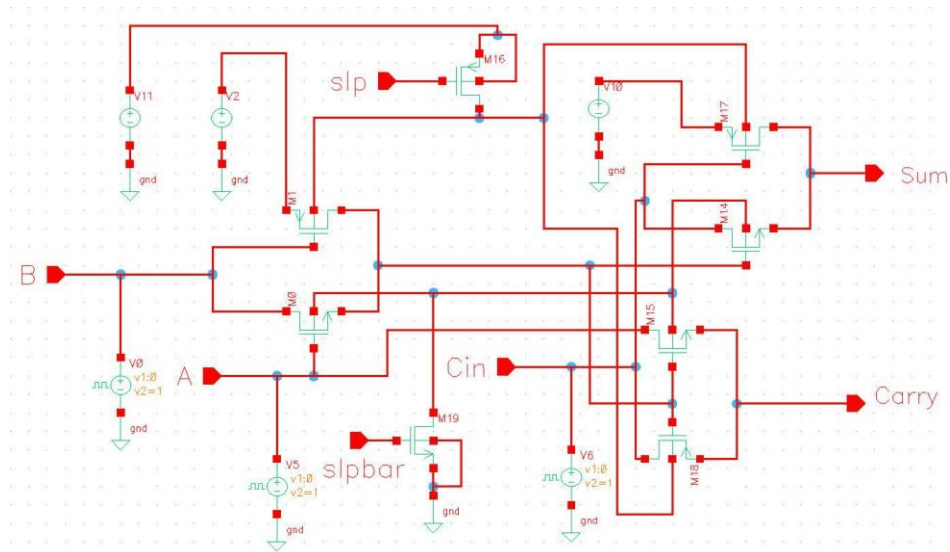


Figure 6. Power gated MGDI full adder

combinational logic circuit known as a full adder takes three input bits-A, B, and Cin- and outputs carry and sum. The demands of consumers for high-speed wireless communication have increased significantly as a result of the development of broadband wireless transmission networks (Dhanasekar *et al.*, 2023a; 2023b).

The adder cell receives the three inputs of the full adder as well as the generated test vectors. The detection of cell delay occurs when the input achieves 50% of the supply voltage until the final carry and sum reach the necessary voltage levels (Morgenshtein *et al.*, 2010). There are eight input pattern combinations: 000, 001, 010, 011, 100, 101, 110, and 111. All transitions between these input combinations have been examined, and the latency for each transition has been determined (Kishore and Sakthivel, 2017).

Proposed Power Gating Based Mgdi Full Adder

The power-gated MGDI complete adder circuit design uses a modified process of GDI and MGDI. The MGDI full-adder has two expressions: Sum and Carry. Compared to the traditional adders' circuits, GDI, and MGDI full adders attain less power and area in the logical circuits. However, the power-gated MGDI full adder design is the best method to achieve optimized area and power in the digital circuits. This full adder operation has three inputs and two outputs namely A, B, Cin, and carry and sum.

Figure 6 shows the schematic for the power-gating MGDI full adder. The circuit uses PMOS and NMOS transistors as well as ports like VDD and GND, output and input pins, and so on. Compared to other methods, power-gated MGDI is unique. It does not produce a strong 1 and a strong 0 as the output step of the GDI approach. Looking for new customized ways to combat these GDI cell drawbacks is preferable. Because of improper biasing at the bulk end, this circuit exhibits a threshold drop. Power gating MGDI full adder is useful for creating high-speed, low-power circuits with fewer transistors. The MGDI design has the benefit of increasing the output swing voltage. Moreover, it allows top-down designs. When the GDI complete adder circuit employs power gating technology, power is switched off when the circuit is latched. In this instance, the circuit power dissipation can be minimized.

Result and Discussion

A Virtuoso physical design tool using 45 nm CMOS technology has been employed to design and implement the proposed power-gated modified gate diffusion full adder.

Performance Measures of GDI Technique using Full Adder

A GDI Full-adder has two outputs (sum and carry), and three inputs (A, B, and Cin). Finally, the result is generated by applying an input voltage

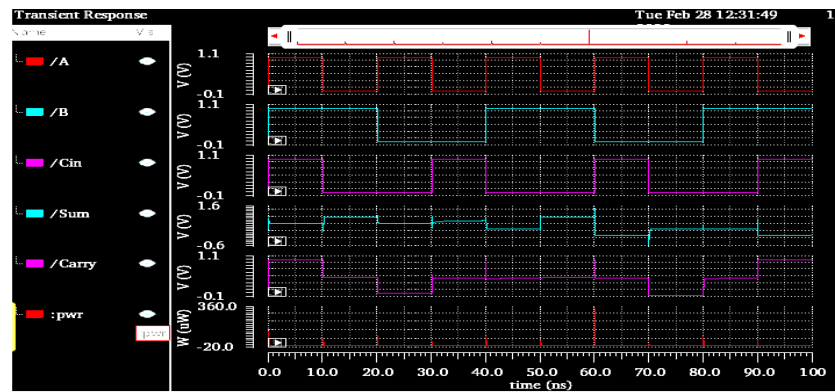


Figure 7. GDI output for full adder

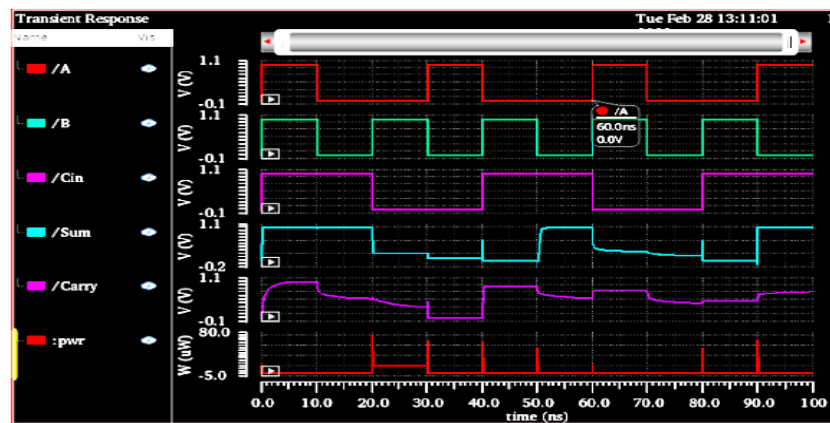


Figure 8. MGDI output for full adder

of 1V, and the transient response is depicted in Figure 7.

The XOR (exclusive OR) combines the three inputs (A, B, and Cin), and generates the sum output. The AND, OR, and NOT gates are used to generate the carry output. It's the result of two AND operations followed by an OR operation. The power obtained as output in a GDI full-adder refers to the electrical power consumed or dissipated by the circuit. Transistor switching and connectivity are the primary factors of lower power consumption in digital circuits such as the GDI full-adder.

Performance Measures of MGDI Technique using Full Adder

A MGDI Full-adder also has two outputs (sum and carry), and three inputs (A, B, and Cin). The simulation result with input voltage of 1V, and the transient response is shown in Figure 8.

The MGDI logic has benefits in terms of lower power consumption and transistor count when compared to traditional digital circuits. The simulation results illustrate the MGDI full-adder

circuit functions, accurately generating carry and sum outputs for every combination of inputs. Additionally, power analysis reveals that the MGDI design attains optimized power than traditional full-adder designs. The efficiency of the proposed design makes it suitable for integration into low-power digital systems.

Performances Measures of Power Gated MGDI Technique using Full Adder

The power-gated MGDI Full-adder also has two outputs (sum and carry), and three inputs (A, B, and Cin). The simulation waveform with input voltage (VDC) of 1V, period of 20 ns rise and fall time will be 1ps, pulse width is 10 ns respectively, and Figure 9 depicts the transient response.

The waveform will show how the voltage of each input changes over time. In this case, with a voltage (VDC) of 1V, a period of 20 ns, and rise and fall times of 1ps, the waveform will reflect these characteristics. For example, rising edges and falling edges will be smooth with a rise and fall time of 1ps, and the voltage will oscillate between 0V and

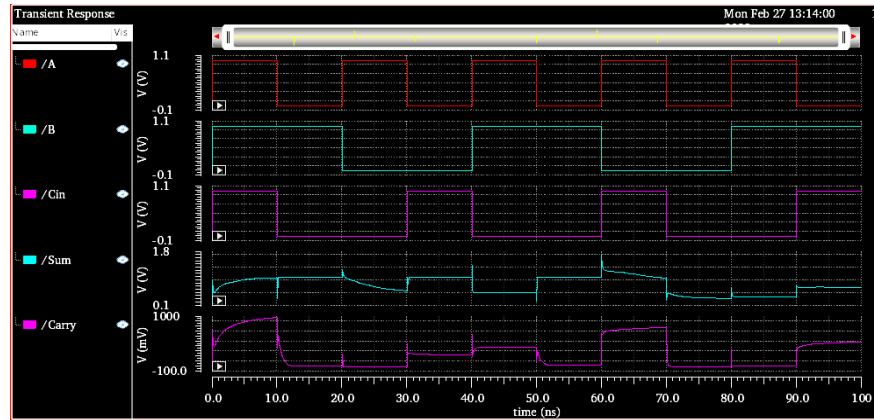


Figure 9. Power gated MGDI output for full adder

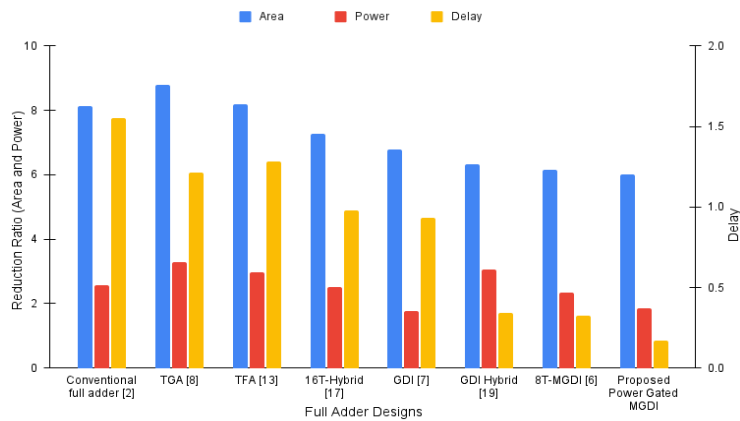


Figure 10. Graphical display of several full adder results regarding area, power, and delay

Table 2. Performance measures of several full adders

Full Adder Designs	Power (pW)	Energy (aJ)	Delay (μ s)	EDP (yJs)	Area (μ m ²)	Transistor Count
Conventional full adder (Navi <i>et al.</i> , 2009)	2.568	3.98	1.55	6.169	8.13	28
TGA (Shams <i>et al.</i> , 2002)	3.277	3.975	1.213	4.821	8.18	20
TFA (Alioto <i>et al.</i> , 2007)	2.98	3.829	1.285	4.927	6.67	16
16T-Hybrid (Bhattacharyya <i>et al.</i> , 2015)	2.506	2.451	0.978	2.397	7.27	16
GDI (Lee <i>et al.</i> , 2007)	1.665	5.494	3.3	18.131	4.93	10
GDI Hybrid (Sanapala and Sakthivel, 2019)	3.053	1.05	0.344	0.361	6.32	14
8T-MGDI (Tejaswini <i>et al.</i> , 2020)	2.351	1.21	0.323	0.390	6.14	8
Propose Power Gated MGDI	1.851	1.05	0.173	0.181	6.023	8

1V with a period of 20 ns. Each waveform will exhibit characteristics such as rising edges, falling edges, stable states, and transitions. The rising and falling edges will be smooth due to the specified rise and fall times. The stable states will show when the input signals stabilize and when the output signals settle to their final values after computation.

Table 2 exhibits comparison results for several Full adder architectures. The proposed full adder has been implemented using the 45 nm CMOS

technology cadence tool. Figure 10 shows the proposed power gating MGDI full adder in comparison to five alternative full adder designs in the literature based on performance measures. The proposed MGDI full adder reduces power

consumption by 96% and delay by 89.5% compared to the Full adder design (Lee *et al.*, 2007). The proposed design improves performance by 50% while consuming 87.6% less power than the existing

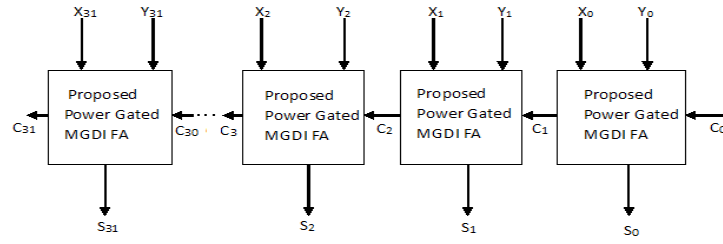


Figure 11. Proposed power-gated based 32-bit carry propagation adder

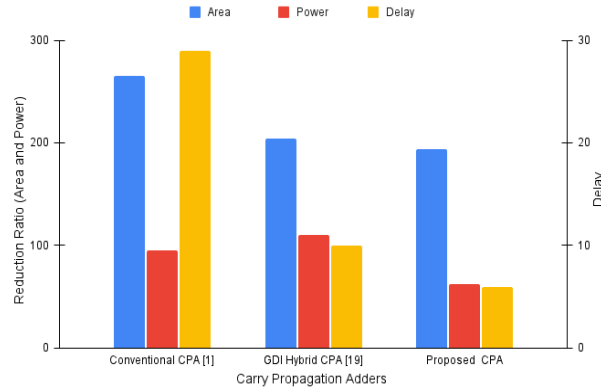


Figure 12. Performance measures for area, delay and power of the existing and proposed 32-bit carry propagation adders

Full adder architecture (Govindaraj *et al.*, 2024). Furthermore, it achieves 83.6% less power usage and a 93% delay in comparison to the full adder (Alioto *et al.*, 2007). The MGDI power gating full adder reduces 78.8% gate count and 17.9% delay compared to the Full adder (Zimmermann and Fichtner, 1997).

The performance measures of several full adders are shown in Table 3. The proposed power-gated full adder provides a conservative performance increase with 27.2% less power and saves 4.02% of the area compared with the conventional full adder (Navi *et al.*, 2009). The proposed adder has a gate delay of 1.55 μ s, which is 88.8% faster than the full adder (Navi *et al.*, 2009). It also consumes 43.5% less power, operates 85.9% faster, and conserves 26.3 of the area than the conventional adders (Shams *et al.*, 2002). This identical adder saves 37.9% power, operates 9.7% less area, and has 86.5% quicker speed relative to the adder (Alioto *et al.*, 2007). The same full adder uses 26% less power, 17% less area and an 82.3% quicker speed than the existing full adder (Bhattacharyya *et al.*, 2015).

The chart displayed in Figure 10 projects the effectiveness of the implementation metrics for the full compressor. The area and power decreased by

Table 3. The truth table for MGDI full adder

N	SN	P	SP	G	D	Function
0	0	1	1	A	A'	INVERTER
A	A	0	A	B	AB	AND
1	0	A	D	B	A+B	OR
A'	0	A	1	B	A'B+A'B'	XOR
A	0	A'	1	B	AB+A'B'	XNOR
0	0	B	B	A	A'B	FUNCTION 1
B	0	1	1	A	A'+B	FUNCTION 2
C	0	B	1	A	A'B+AC	MUX

4.7% and 39.3%, respectively, by using the same full adder as the traditional full adder (Sanapala and Sakthivel, 2019). The proposed full adder also reduces 21.2% power, operates 46.4% faster and attains 97% EDP with the same transistor count as 8 (Tejaswini *et al.*, 2020). In addition to the existing adder, the full adder performs 94.8% faster (Lee *et al.*, 2007). Hence, an area and power-efficient full adder design has been attained and it is used for carry propagation adder.

Performance Measures of Carry Propagation Adder

The proposed power-gated MGDI full adder's performance has been evaluated using the carry propagation adder design depicted in Figure 11.

A 32-bit carry propagation adder is generated by cascading the proposed power-gated 1-bit adder. In this case, carry propagation occurs from the first to the final adder block.

Table 2 shows the performance metrics of various 32-bit carry propagation adders. To evaluate the carry propagation adder's effectiveness, an extensive evaluation has been carried out. The proposed 32-bit carry propagation adder is implemented using the 45 nm CMOS technology cadence tool. In comparison to the existing propagation adder, the proposed propagation adder decreases delay by 65.5% and uses 34.5% less power and 26.9% less area (Sanapala and Sakthivel, 2019). Figure 12 shows the implementation metrics for the proposed 32-bit carry propagation adder.

In comparison to the traditional adder, it also achieves 5.1% less area, 43.3% less power, and 40.9% faster speed (Sanapala and Sakthivel, 2019). In comparison to the conventional adder, the proposed 32-bit carry propagation adder performs better in terms of area, delay and power.

Conclusions

The power-gated MGDI full adder proposed in this research article is intended to be used for a 32-bit carry propagation adder. The same full adder has been implemented using a 45nm CMOS cadence tool. In the proposed full adder, the delay was reduced by 46.4% and the power consumption was reduced by 21.2%. The 32-bit carry propagation adder uses a power-gated 1-bit full adder, which occupies less area and optimized power than the conventional adders. Therefore, the proposed power-gated-based MGDI full adder can be used for higher-bit adder architectures, thereby reducing power consumption and area.

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