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Group maximum power tracking for distributed power source

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Abstract

This paper offers a useful application of Uniform Input Voltage Distribution (UIVD) control for Distributed-Input Parallel-Output (DIPO) converter power systems. The primary control objective of UIVD for DIPO converters is to achieve grouped maximum power throughput from non-identical renewable power sources. Secondly, this paper features a revised Maximum Power Tracking (MPT) controller design developed for DIPO configurations that facilitate simultaneous processing of distributed power flows. In earlier research, the distributed source peak powers are individually tracked by converters controlled by independent MPT controllers without UIVD. However, when distributed power sources have similar peak power voltages with an achievable tracking efficiency of greater than 96%, such independent MPT controllers are not necessary. By utilizing UIVD control, near-maximum use of available power is achieved using a single MPT controller. The resulting system and control architectures offer near-maximum power transfer with a lower parts count. Two DIPO power converter bus architectures are described herein: one having a battery-dominated output voltage and the other with a regulated output voltage. Through computer simulation and prototype testing, both power architectures are validated for fault-tolerant grouped UIVD control.

Keywords: *power converter, maximum power tracking*

1. Introduction

Reliable and expandable power architectures and control approaches enable efficient power processing from distributed and unregulated power sources to a commonly usable and well-regulated voltage. Distributed-input parallel-Output (DIPO) configured converter power systems are becoming a viable choice (Siri & Conner, 2001; Siri & Conner, 2002; and Siri & Conner, 2003) for achieving reliable power/voltage performance in aerospace and renewable energy applications. For DIPO converters to achieve optimum power throughput from non-identical power sources, UIVD control is utilized herein. This paper introduces the unconventional use of a single MPT controller combined with UIVD control developed for a DIPO converter architecture, which simultaneously processes distributed flows of electricity with outstanding fault tolerance. Through modeling, simulation, and prototype testing, this paper demonstrates that nearly full utilization of energy delivered by the distributed sources having non-identical peak power ratings can be achieved through a unified integration of MPT and UIVD control. Two power system architectures are studied in this paper; one is a battery-dominated bus while the other is a regulated-voltage bus. Because of UIVD control, group maximum utilization of distributed power sources is accomplished using one MPT controller rather than independent MPT controllers, each of which is conventionally dedicated to its respective power source.

Previous studies (Siri, Truong, & Conner, 2005; Siri & Willhoff, 2007; and Siri, Willhoff, & Conner, 2007) of series-input parallel-output (SIPO) converter architectures revealed how UIVD control can achieve uniform power sharing among series-connected converters that absorb identical DC input currents. However, instead of power processing from a common power source, UIVD control adopted in SIPO converter architectures was designed (Siri & Willhoff, 2011) to achieve optimum power throughput from series-connected power sources. Because different peak powers exist among non-identical power sources, near-maximum utilization of all the power sources is still achievable by applying UIVD control as long as the peak power voltages of the individual sources are similar or

mismatched within an acceptable tolerance (such as ± 20%). UIVD serves as a cost-effective method of power management and distribution for SIPO converters having similar peak-power voltages.

Earlier studies (Siri and Conner, 2001; Siri and Conner, 2002; and Siri and Conner, 2003) of DIPO converter architectures also demonstrated the feasibility of using independent maximum power tracking (IMPT) controllers dedicated to each respective converter for regulating power flow from each distributed source without UIVD. The peak powers delivered from the distributed power sources are independently tracked by the respective converters that are controlled by the respective independent MPT controllers. However, when distributed power sources have similar peak power voltages and a tracking efficiency of at least 96% is expected, independent MPT controllers are not necessary. Demonstrated herein is a single MPT controller, which was previously studied through modeling and simulation with SIPO converter architectures (Siri and Willhoff, 2011) for tracking a system's optimum power point using DIPO converters with UIVD control to support optimum power flows from distributed power sources. Each distributed power source is independently connected across the input port of its respective converter. For non-identical power sources, the unified MPT/UIVD system controller enables optimum power transfer from distributed power sources over uniform power sharing among DIPO converters. Section 4.3 illustrates that DIPO converter architecture combined with UIVD and group MPT controller can tolerate multiple short-circuit faults across converter inputs. Furthermore, the revised MPT controller design is less complex than those MPT controllers used in the previous studies (Siri and Conner, 2001; Siri and Conner, 2002; and Siri and Conner, 2003). Section 2.1 will also introduce a novel system controller that offers regulation of the distributed input voltages using Maximum-Limit (ML) voltage feedback together with UIVD control to regulate the distributed source voltages at a system optimum-power voltage regardless of induced short-circuit faults. During fault conditions, the system optimum-power voltage is controlled for the remaining functional sources from which the total source power is kept as close as practical to the summation of the remaining functional ideal peak powers.

2. Converter power system description

Figure 1 depicts an output-isolated DC-DC converter with an opto-coupler circuit that provides electrical isolation for controlling the converter power flow using the control input V_{Ci}. In this manner, many isolated-control converters can have their input power ports individually connected to their respective power sources, while the converters are independently controllable through their respective control inputs (V_{Ci}). Their outputs are connected in parallel for power delivery to a shared load. In general, each converter's input-power return, -IN, and the system controller's reference ground may not have the same operating voltage or are not in the same electrical node. Therefore, isolated-control converters with their respective opto-coupler circuits provide flexibilities for interconnection among many converters such that their input power returns do not need to be tied together to the system controller's reference ground. Typically, an input-filter capacitor (C_{IN}) of sufficient capacitance is terminated across each converter input to achieve an acceptable AC input-ripple voltage, particularly when the converter input voltage is controlled to meet certain control objectives.

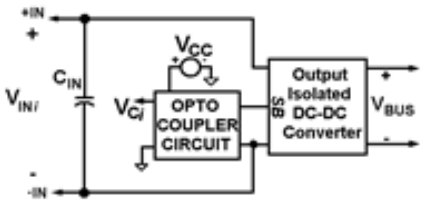

Figure 1 Basic DC-DC converter with an opto-isolated control input V_{Ci} that is electrically isolated from the converter's input power and return terminals.

Each isolated-control DC-DC converter shown in Figure 1 can be a single-converter power stage or a group of multiple-converter power stages that are connected in parallel. These parallel-connected converter power stages of a current-mode type are preferred. The current-mode converter power stages allow for a common shared-bus voltage signal to command these converter power stages in unison to achieve uniform current-sharing and at the same time to serve other control objectives. Different approaches of shared - bus current-sharing were studied for parallel-connected

converters of current-mode type (Siri, 1999) and for those of non-current-mode type (Jordan, 1991-1996). According to these studies, some current-sharing control schemes are not able to realize the commonly controllable current-sharing shared-bus such as the scheme published by Jordan (1991-1996) since the parallel-connected converter power stages are not of the current-mode type, and its shared-bus can only be used for current-sharing purposes and cannot be controlled directly to serve other control objectives.

2.1 Battery-dominated power system

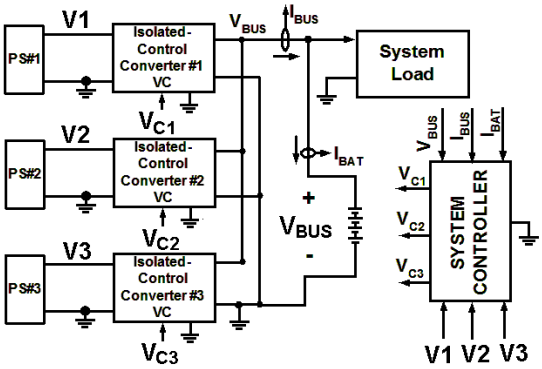

Figure 2 Battery-dominated *3*-converter DIPO power system with 3 distributed power sources

Figure 2 illustrates a DIPO converter power system architecture consisting of three distributed-input converters with their outputs connected in parallel across a battery bank having an output voltage V_{BUS}. A system load may be terminated across the output voltage that becomes a battery-dominated voltage bus. Each of these three isolated-control dc-dc converters shares the following attributes: (a) includes a shared-bus control input SB*i*, which allows an external signal to take control of the converter power stage; (b) may represent a number of parallel-connected converter modules configured with shared-bus control inputs tied together to form a common shared-bus control port so as to achieve nearly uniform current-sharing; (c) may operate in a stand-alone configuration wherein the output is regulated at a pre-determined voltage and its shared-bus input is left unconnected; and (d) must provide electrical isolation between input and output. There are six feedback input signals feeding the system controller shown in Figure 2, which are the battery-bus voltage V_{BUS}, the system bus current I_{BUS}, the charging battery-bank current I_{BAT}, and the distributed input voltages V1, V2, and V3 of the three independently sourced converters. Figure 3 depicts a conceptual block diagram of the system controller employed in the battery-dominated power architecture shown in Figure 2. The system controller provides four basic control functions: (1) system battery charge control, (2) system distributed input-voltage regulation, (3) uniform input voltage distribution (UIVD), and (4) system maximum power tracking (MPT). The DIPO converter system may include a bus stabilizer network terminated across the system output V_{BUS} located as close to the system output port as possible to damp out ac energy, thus ensuring system stability.

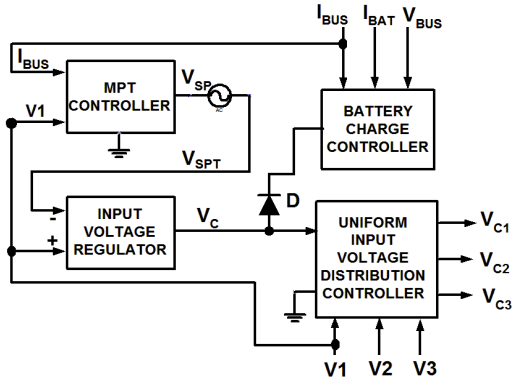

Figure 3 UIVD controller for DIPO converter power system

Typically, the battery charge controller shown in Figure 3 regulates the battery-bank voltage V_{BUS} to a preset value in accordance with its voltage-temperature (V/T) profile in order to prevent battery over-charging. When the battery-bank voltage V_{BUS} is below its preset value that is pre-assigned as a function of temperature, the battery-bank current I_{BAT} is regulated at a preset charge-current set-point determined by the charge controller. Active battery regulation of either its voltage, V_{BUS}, or charge current, I_{BAT}, leads to a forward-voltage bias across the pull-down diode, D, shown in Figure 3. However, when V_{BUS}'s voltage and I_{BAT}'s current are respectively below the preset voltage value and the preset charge-current set-point, the system controller regulates the system distributed-input voltage, V1, at the optimum peak-power voltage that is determined by the MPT control. As long as the operating battery-bank voltage and current are below their preset voltage/charge-current values, the DIPO converter power system is controlled to have an

optimum power transfer from all distributed power sources. This is achieved by utilizing only one MPT controller that dominates its control over the battery charge controller through the primary control signal V_C and the reverse-biased diode, D. Only one of the following three operational modes is active at a time - battery voltage regulation mode for compliance with a V/T profile, battery charge-current regulation mode for charging the battery at a commanding charge rate, or distributed-input voltage regulation mode for tracking a system optimum-power voltage. During any of these three operating modes, converter-input voltages across the distributed power sources are always regulated to be equal by the UIVD controller that properly distributes three control voltage signals V_{C1}, V_{C2}, and V_{C3} to their respective isolated-control converters #1, #2, and #3.

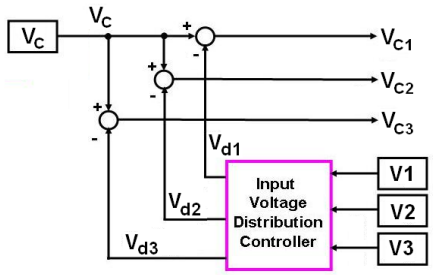

Figure 4 Uniform input voltage distribution controller block diagram for 3 DIPO converters.

In general, a DIPO power system may consist of *N* isolated-control DC-DC converters with their respective *N* series-connected power sources PS#1, PS#2, . . . , PS#*N*. During either the battery voltage/current regulation or the distributed-input voltage regulation, the converter-input voltage distribution controller as shown in Figure 4 produces secondary control signals (V_{d1}, V_{d2}, . . . , V_{dN}). The secondary control signals are subtracted from the primary control voltage, V_C, to create a modified control voltage (V_{C1}, V_{C2}, . . . , V_{CN}) that regulates its respective converter to accomplish uniform input voltage distribution. A common distributed reference signal, $V_{DIS} = V_1/N$, serves as the central-limit (CL) distribution reference (Siri and Willhoff, 2012), where N=3 is the number of distributed converters. The voltage difference between V_{DIS} and each converter-input voltage (V_1, $V_{2\,,\,.\,.\,.\,,}V_N$) is amplified, frequency-compensated, and finally output as the voltage distribution control signal (V_{d1}, $V_{d2,\ .\ .\ ,}$ and V_{dN}, respectively). Each secondary control signal, V_{di}, provides a minor control correction to the primary control voltage, V_C, thus ensuring uniform input voltage distribution.

The UIVD controller is not fault-tolerant when the common distributed reference signal, $V_{DIS} = V_1/N$, is the central-limit (CL) distribution reference. If one converter fails and cannot be controlled due to a short circuit across its input, the system will lose regulation. Figure 5 shows the improved UIVD controller that is based on the Maximum-Limit (ML) distribution reference, $V_{DIS} = MAX(V_1, V_{2\,,\,.\,.\,.\,,}V_N)$. To achieve fault-tolerance, a set of ideal rectifiers is included as part of the UIVD controller to produce a common distributed voltage reference signal, V_{DIS}, which is the highest output voltage obtained from one of the converters within the power system. Therefore, if a converter fails with its input short circuited, V_{DIS} is automatically increased to compensate for the loss of a failed converter or the failure of its respective input power source. For the system to tolerate at least one converter input short-circuit failure, two ideal rectifiers are required to sense the output voltage from any two converters. Up to *N* ideal rectifiers are included in the UIVD controller for an *N*-converter DIPO system.

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Consequently, Figure 5 illustrates the UIVD control for an *N*-converter DIPO power system with fault-tolerance. A common distributed

voltage reference signal, V_{DIS}, is derived from *N* cathode-parallel-connected ideal rectifiers so as to individually sense the input voltages of converters #1, #2, . . . , and #*N*. If one converter fails to build up its input voltage, the *N*-1 remaining converters will be controlled to have uniform input voltage distribution. The *dc* gain for each voltage distribution error amplifier shown in Figure 5 does not need to be high in order to achieve uniform input voltage distribution. On the contrary, high *dc* gain within each distribution error amplifier causes the converter-input voltage distribution controller to dominate the battery charge control and the distributed-input voltage regulation modes of operation, resulting in insufficient charging to the battery bank.

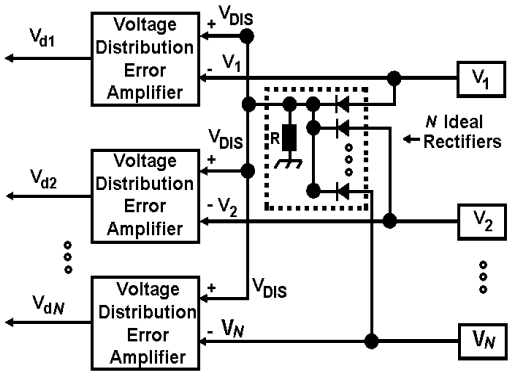

Figure 5 Fault-tolerant uniform input voltage distribution controller using the Maximum-distribution reference

2.2 Regulated-bus power system

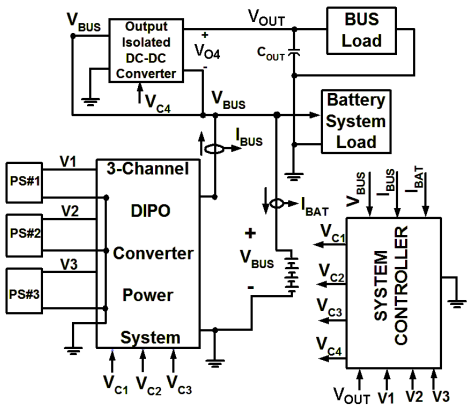

Figure 6 Dual-regulated bus power architecture with UIVD control

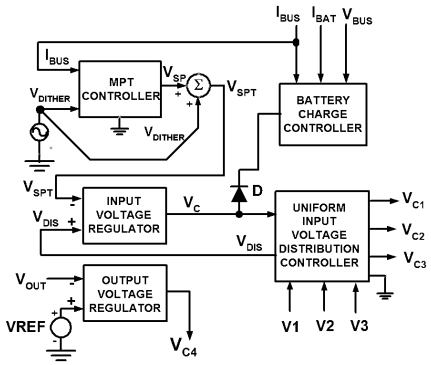

Figure 7 System controller for the dual regulated buses employed in the system

Figure 6 shows another DIPO converter power system architecture consisting of three independently sourced input -converters with their outputs that are connected in parallel across a battery bank having an output voltage V_{BUS}. A system load may be terminated across the battery voltage V_{BUS} which serves as a battery-dominated voltage bus. Each of these three isolated-control dc-dc converters share the same four attributes previously described for Figure 2. There are seven feedback input signals feeding the system controller shown in Figure 6: the battery-bus voltage V_{BUS}, the regulated-bus output voltage V_{OUT}, the system battery-bus current I_{BUS}, the charging battery-bank current I_{BAT} , and the distributed input voltages V1, V2, and V3 of the distributed-input converters. Figure 7 depicts a conceptual block diagram of the system controller employed in the dual-bus power architecture shown in Figure 6. The system controller provides five basic control functions: (1) system output voltage regulation of V_{OUT}, (2) system battery charge control, (3) input voltage regulation of the distributed input voltages V1, V2, and V3, (4) uniform input voltage distribution (UIVD), and (5) system maximum power tracking (MPT). In the same manner, a bus stabilizer network may be terminated across the system output V_{OUT} located as close to the system output port as possible to damp out ac energy, thus ensuring system stability. The system regulated-bus voltage V_{OUT} is closed-loop controlled by an output-isolated DC-DC converter with its output port V_{O4} that is series-connected with the battery-bus voltage V_{BUS}. This special output-series-connected converter significantly improves the system efficiency since the converter output voltage V_{O4} can be a minor portion of the overall output voltage V_{OUT}, and the battery voltage V_{BUS} can be

the major portion. The control signal V_{C4} drives the converter's power stage to regulate the V_{OUT}'s voltage at a fixed value above the system battery-bus voltage V_{BUS}. The system controller shown in Figure 7 provides a much more fault-tolerant coverage than the system controller shown in Figure 3 since the input voltage regulator controller has the distribution voltage V_{DIS} as its feedback input instead of the PS#1's voltage V1. Since V_{DIS} is the maximum-limit voltage that is the maximum sourcing voltage detected from those of the three power sources or V_{DIS} = MAX(V1, V2, V3), the input voltage regulator provides active control on V_{DIS} to follow the commanding set-point voltage V_{SPT}. There always exists one converter's input voltage that is the highest among all the distributed-input voltages while they are controlled to have a uniform distribution at all times. This maximum-limit input voltage regulation allows the DIPO converter system to tolerate more than one failure due to the short-circuit or open-circuit of power sources and/or short-circuit or overload across distributed inputs of DIPO converters.

3. Simulation of DIPO power systems

3.1 Regulated-bus power system simulation

A PSPICE model of the regulated-bus power system with three DIPO converters and three distributed power sources, as shown in Figure 6, was simulated to verify the basic functionality of its control loops. Bus output voltage regulation was added into the system for regulating the bus voltage V_{OUT} at 28 VDC. The single-MPT control with UVD ensures the continuously updated solar array set-point voltage, V_{SPT}, which commands the input-voltage regulation control loop to regulate the distributed input voltages, V1, V2 and V3 at the group peak-power voltage of 32.2 VDC.

Figure 8 illustrates the simulated response of the system output bus voltage, V_{OUT}, in the bottom plot, and the distributed-input voltages, V1, V2, and V3, depicted as three overlapping traces in the middle plot. V_{OUT} is well regulated at 28 VDC at all times despite a 28-A step-load, shown as a "system load current" trace on the bottom plot. The 28-A step-load causes the battery charge current to drop from 50.08 A to 14.3 A at time t = 15 s since the single-MPT controller still tracks the group peak-power voltage, V1= 32.2 VDC without loss of UIVD control.

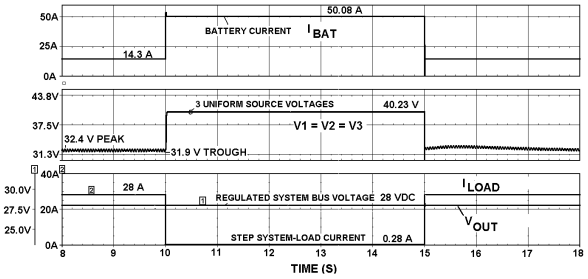

Figure 8 Simulated response of the three input voltages and the system regulated bus voltage V_{OUT} for the power system shown in Fig. 6 with GT-UVD control during a 784-W step-load across the bus voltage V_{OUT}

3.2 Simulation of system fault-tolerance

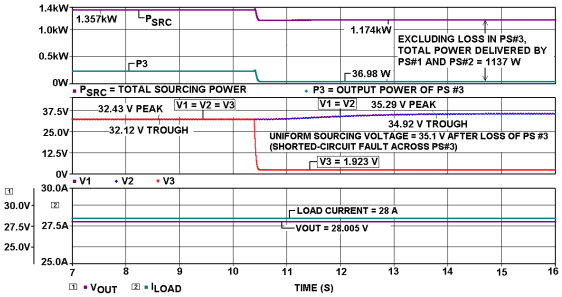

Figure 9 Simulated response of the distributed source voltages, total sourcing power, and the system output voltage V_{OUT} of the power system shown in Figure 6 with GT-UVD control before, during, and after a loss of power source PS#3

Figure 9 depicts another set of simulated responses of the total sourcing power P_{SRC}, the system output bus voltage V_{OUT}, the distributed input voltages V1, V2, and V3, and the load current drawn from the bus voltage as power source PS#3 experiences a short-circuit fault across its terminals, leading to nearly zero voltage across the input of converter #3, V3 = 1.923 V, at time t = 10.4 s. The voltage loss across power source PS#3 causes the system optimum sourcing power (the purple trace on the top plot) to drop from 1357 W to 1137 W and the two remaining distributed peak-power voltages, V1 and V2, to increase from 32.275 V to 35.105 V (the middle plot). The system output voltage V_{OUT} (the blue trace on the bottom plot) is still well regulated at 28 VDC at all times despite the reduction in the total system peak power since the load power of 784 W @ load current of 28 A as shown in the purple trace on the bottom plot is still significantly below

the reduced system peak power of 1137 W. The single-MPT controller, while maintaining the tracking of the peak-power voltage without loss of UVD control, also regulates the AC ripple voltage superimposed on the operating peak-power voltage.

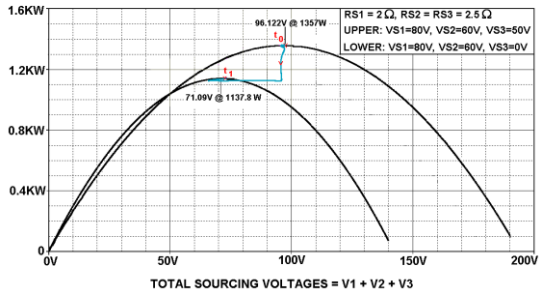

Figure 10 Simulated P-V trajectory of the net delivered power as a function of the total sourcing voltage as shown in blue, for the power system shown in Figure 6 with single-MPT control before, during, and after a loss of power source PS#3; the trajectory is overlaid on two static P-V characteristics: the upper one before the loss of PS#3 and the lower one after the loss of PS#3

Figure 10 overlays the simulated trajectory of total sourcing power versus total sum of three distributed sourcing voltages (or the P-V trajectory) on two P-V static characteristics, one of which belongs to three functional power sources (PS#1, PS#2, and PS#3) and the other belongs to two functional power sources (PS#1 and PS#2). The simulated P-V trajectory shown in blue is extracted from the same time-domain simulation results shown in Figure 9, uncovering the change in the system peak power from 1357 W (at starting time t_0) to 1137.8 W (at final time t_1). These two power levels are very close to their respective peak power points on the two P-V characteristics.

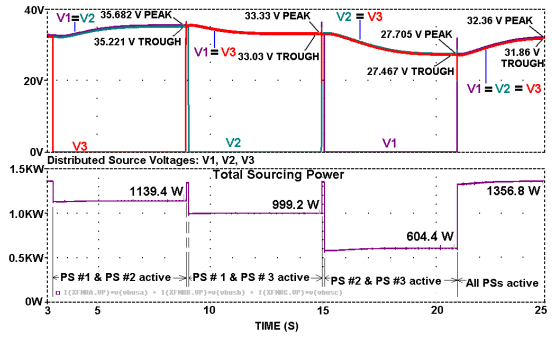

Figure 11 Simulated response of the distributed source voltages and total sourcing power of the power system shown in Figure 6 with GT-UVD control during a loss of each power source at a time

Figure 11 reveals the simulated response of the same power system shown in Figure 6 to demonstrate the effectiveness of UVD control despite a total power loss of any power source within the system. The bottom plot in the figure shows the system's available sourcing power when only the two remaining power sources are still functioning, delivering the system sourcing peak power of 604.4 W, 999.2 W, and 1139.4 W, respectively, when the power system may lose one power source PS #1, PS #2, and PS#3 accordingly. During a total power loss of one power source, the system peak power voltages for the two remaining functioning sources are autonomously adjusted to new optimum power voltages; 27.58 V, 33.18 V, and 35.45 V, respectively, after a loss of the corresponding power sources PS#1, PS#2, and PS#3. And the voltages of the two remaining functional sources are still uniformly distributed as shown in the top plot of Figure 11.

For the same power system shown in Figure 6, Figure 12 discloses simulation result of the sourcing voltages on the bottom plot, the system output voltage on the middle plot, and total sourcing power on the top plot, revealing the tolerance of failures in more than one power source.

For time $8 < t < 9$ s, power source PS#3 fails to deliver power (V3=0), and the two remaining power sources are able to deliver their total sourcing power of 1137 W, resulting in 99.9% of tracking efficiency for power sources PS#1 and PS#2. For time $9 < t < 15$ s, power source PS#2 fails (V2=0), and the two other power sources are able to deliver 997.8 W as their total optimum power, revealing 99.7% of tracking efficiency for power sources PS#1 and PS#3. For time $15 < t < 21$ s, power source PS#1 fails (V1=0), and 604.9 W of the total optimum power is produced from power sources PS#2 and PS#3, demonstrating 99.98 % tracking efficiency. For time $21 < t < 27$ s, two power sources, PS #1 and #3, fail and only power source PS#2 delivers its optimum power of 359.9 W, which is almost the same as the 360-W ideal peak power that PS #2 can offer. As all three power sources are restored to normal after time t = 27 s, they resume 1357 W of the total optimum power. During all of these five simulated scenarios, the system output voltage (the middle plot of Figure 12) is still well regulated at 28 V, and the voltages across any remaining functioning power sources are uniformly distributed as anticipated.

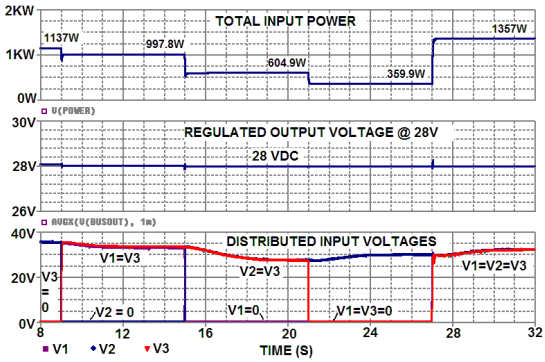

Figure 12 Simulated response of the distributed source voltages, system output voltage, and total sourcing power of the same power system shown in Figure 6 with GT-UVD control before, during, and after (1) only one power source failure at a time from t=9 to 21 s, and (2) two power source failures in tandem (PS#1 and PS#3) from t=21 to 27 s

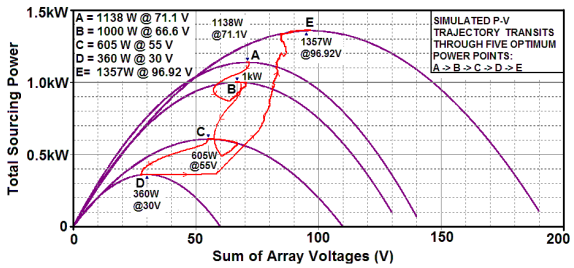

Figure 13 Simulated P-V trajectory of the total sourcing power as a function of the total sourcing voltage as shown in red, for the power system shown in Figure 6 with single-MPT control; the trajectory is overlaid on five static P-V characteristics showing five operating optimum power points: A, B, C, D, and E.

Figure 13 shows the simulated P-V trajectory of power versus total sourcing voltage as shown in red. The simulated P-V response is overlaid on five static P-V characteristics (in purple) having five different peak powers. All the simulation results shown in Figure 13 are extracted from the same PSPICE data file from which the simulated time-domain response is produced, as shown in Figure 12. Regardless of how many power sources experience short-circuit across their sourcing terminals; i.e. a single short-circuit fault or two short-circuit faults or no short-circuit fault, the single MPT control with UIVD is able to achieve over 99 % of tracking efficiency for all five optimum power points (points A, B, C, D, and E).

4. Prototype development and testing

A 3-channel DIPO converter power system prototype was built according to the system block diagram shown in Figure 14, revealing only five feedback signals that serving as the inputs to the system controllers. Three sourcing voltages V1, V2, and V3 remain as the basic feedback signals for the system controller to properly distribute three control signal outputs V_{C1}, V_{C2}, and V_{C3} for equal sourcing voltages. The system output voltage of the DIPO converters, V_{OUT}, is fed back to the controller so that V_{OUT} is regulated under normal operating conditions, which are considered to be in a non-maximum power tracking (non-MPT) mode. The fifth feedback input is the total sourcing current signal, I_S, which serves as a mandatory signal for computation of the total sourcing power signal.

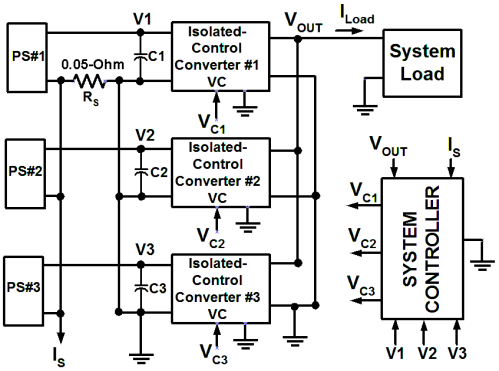

Figure 14 Block diagram of the 3-channel DIPO converter power system including system controller

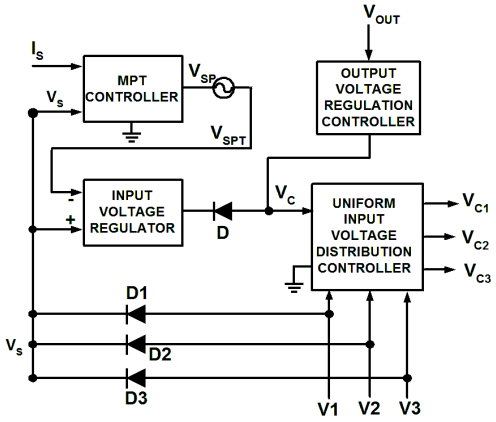

Figure 15 Block diagram of the system controller developed for the prototype shown in Figure 14

Figure 15 depicts the internal block diagram of the system controller that provides all essential control functions for proper operation of the DIPO converter power prototype. Four basic control functions are implemented in the power system prototype: (1) output voltage regulation (OVR), (2) identification of a maximum-power voltage candidate through the MPT controller, (3) input voltage regulation (IVR), and (4) uniform input voltage distribution (UIVD). Under a non-MPT mode of operation, the OVR controller actively regulates the system output voltage V_{OUT} by properly delivering a primary control signal V_C while the MPT and IVR controllers are in their stand-by mode, which does not interfere with the normal OVR function. Diode D shown in Figure 15 is reverse-biased to prevent conflict between the IVR control and the output voltage regulation since the sourcing voltages under normal OVR mode are above the minimum sourcing voltage corresponding to the stand-by minimum set-point voltage $V_{SP\text{-}MIN}$. Whenever the load demand across V_{OUT} exceeds the system maximum power, the OVR controller loses its active regulation, and the sourcing voltages collapse toward the idle minimum sourcing voltage. The sourcing-voltage collapse triggers the MPT and IVR controllers to engage their control contribution to the primary control signal V_C since diode D becomes forward-biased. In this manner, the forward-biased diode D provides an active pull-down to the system control voltage V_C that is no longer controlled by the OVR controller since the output impedance of the IVR controller becomes significantly less than the output impedance of the OVR controller. When this transition from OVR mode to MPT mode occurs, the set-point voltage V_{SP} starts increasing from its minimum idle voltage $V_{SP\_MIN,}$ which corresponds to the minimum sourcing voltage. Consequently, the maximum-limit sourcing voltage V_S is regulated by the IVR controller to track a voltage value corresponding to V_{SP}. Usually, the maximum-limit sourcing voltage V_S is obtained from the strongest power source among the three distributed power sources through the maximum-limit detection circuit, consisting of three paralleled-cathode diodes D1, D2, and D3. Furthermore, V_S also possesses a low-frequency AC signal content that is in phase with the AC dither signal being superimposed on the maximum-power set-point voltage V_{SP}. The uniform input voltage distribution controller has sufficient gain and control bandwidth such that the sourcing voltages belonging to weak power sources can be regulated to track the sourcing voltage belonging to the strongest power source. According to the UIVD control block diagram shown in Figure 5, the UIVD controller still functions properly even with the presence of a short-circuit fault across any power source because voltages across the remaining functional power sources are controllable to be uniformly distributed or nearly equal. In this manner, the 3-channel power system prototype can tolerate failures in up to two power sources.

The 3-channel DIPO power system prototype is shown in Figure 16, revealing three PCBs: one mother board PCB and two daughter board PCBs. The mother board PCB contains three COTS DC-DC converters, the two controller daughter board PCBs and the house keeping power supply. There are five ports for connections on the mother board to its surrounding subsystems: three input ports for three distributed input power sources, one output port for load circuitry, which consists of an electronic load and a decade resistor load box, and one signal input port for a 110-VAC 60-Hz signal that serves as the dither signal.

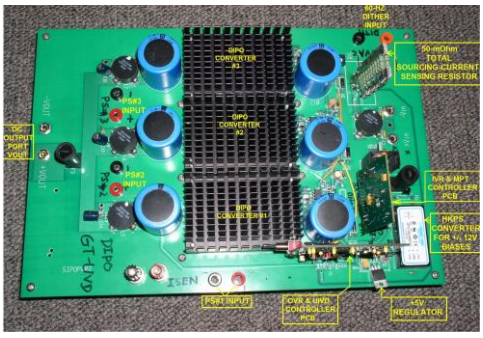

Figure 16 Photo of 3-channel DIPO converter power prototype showing three PCBs: one power PCB, and two controller PCBs

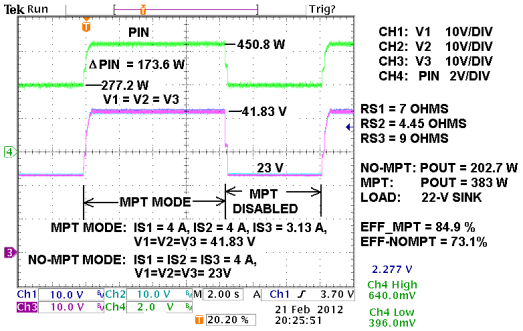

Figure 17 Prototype response during an MPT mode of operation and a disabled MPT mode of operation

Figure 17 depicts the prototype response that demonstrates both enabled and disabled MPT modes of operation including their mode transitions. Each of the three input power sources were designed to have current limited at 4 A. This is to prevent the electronic load from absorbing excessive output power. The load was set to be a 22-VDC constant voltage sink to represent a battery load. When the MPT mode is enabled, the DIPO converter power system absorbs 450.8 W of total input power, delivers 383 W output power, and sustains the uniformly distributed sourcing input voltages of 41.83 VDC. The enabled MPT mode of operation helps the DIPO power system operate in their typical input voltage range, which ensures normal power conversion efficiency of 84.9%. When the MPT mode is disabled, the power prototype absorbs only 277.2 W of total input power, delivers only 202.7 W output power into the constant voltage sink load, and sustains the uniformly distributed sourcing input voltages that are collapsed to a significantly lower voltage of 23 VDC. Without MPT control, the three DIPO converters cannot maintain their input voltages within their acceptable input voltage range (36 – 72 VDC), leading to not only the far- from-optimum power throughput but also the poor power conversion efficiency of only 73.1 %.

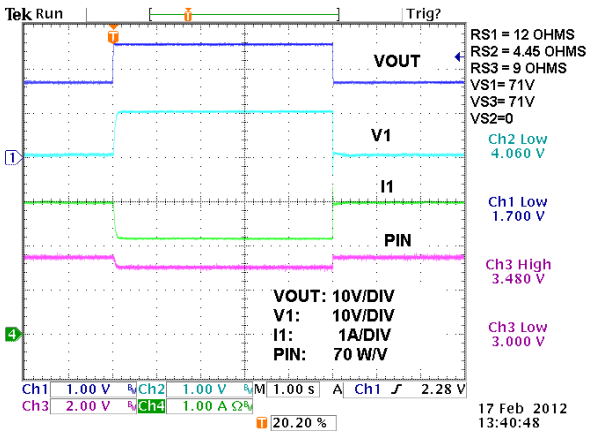

Figure 18 Transitions between OVR mode and MPT mode with two active sources PS#1 and PS#3: P_{IN} = 243 W in MPT mode, and P_{IN} = 210 W in OVR mode

Figure 18 shows the prototype's response when the system load steps between a heavy and a nominal load, causing the system control to operate between MPT and OVR mode, respectively. Only power sources PS#1 and PS#3 are active (their open-circuit voltages: VS1= VS3 = 71 VDC) and PS#2 is inactive (VS2 = 0). Under a heavy load, the system output voltage loses its regulation (V_{OUT} = 17 VDC) and the system controller operates in MPT mode to allow the power system to absorb the optimum input power of 243 W while the distributed sourcing voltages, V1=V3, are optimally equal at 40.6 VDC. Under a nominal load, the system controller operates in OVR mode, and the output voltage is regulated at around 25 VDC with the total input power of 210 W. The oscilloscope waveforms shown from top to bottom are the system output voltage, the PS#1 input voltage, the PS#1 input current, and the total sourcing input power, respectively.

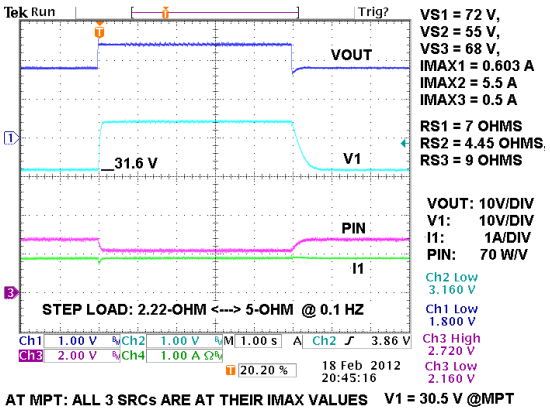

Figure 19 Transitions between OVR mode and MPT mode with 3 active sources PS#1, PS#2, and PS#3: P_{IN} = 190.4 W in MPT mode, and P_{IN} = 151.2 W in OVR mode

Figure 19 shows the prototype's response when the system load steps between 2.22 and 5 Ω at 0.1 Hz, causing the system control to operate between MPT and OVR mode respectively. All three power sources PS#1, PS#2, and PS#3 are active (their open-circuit voltages: VS1 = 72 V, VS2 = 55V, VS3 = 68 V). Under the 2.22-Ohm load, the system output voltage loses its regulation (V_{OUT} = 18 VDC) and the system controller operates in MPT mode to allow the power system to absorb the optimum input power of 190.4 W while the distributed sourcing voltages, V1=V2=V3, are optimally equal at 31.6 VDC. Under the 5-Ω load, the system controller operates in OVR mode and the output voltage is regulated at around 24 VDC with the total input power of 151.2 W. The oscilloscope waveforms shown from top to bottom are the system output voltage, the PS#1 input voltage, the total sourcing input power, and the PS#1 input current, respectively.

Figure 20 shows the prototype response of the three input sourcing voltages (V1 in dark blue, V2 in light blue, and V3 in pink) and the total sourcing input power (in green trace) during the MPT mode of operation, revealing gradual transitions from a state of three active power sources to a state of two active power sources PS#2 and PS#3, and finally to a state of one active power source PS#2. The gradual inactive power sources demonstrate their possible faulty conditions that do not cause the loss of MPT operation for the remaining active power sources. Figure 20 also reveals two occasions in which the collapse of sourcing input voltages occurs when the MPT operation is disabled. One occasion is on the far left of the figure when three power sources are active with their uniform voltages, and another occasion is on the far right of the figure when only power source #2 is active. In both occasions, the total sourcing input power under the disabled MPT mode is always less than that under the enabled MPT mode for the same number of active power sources.

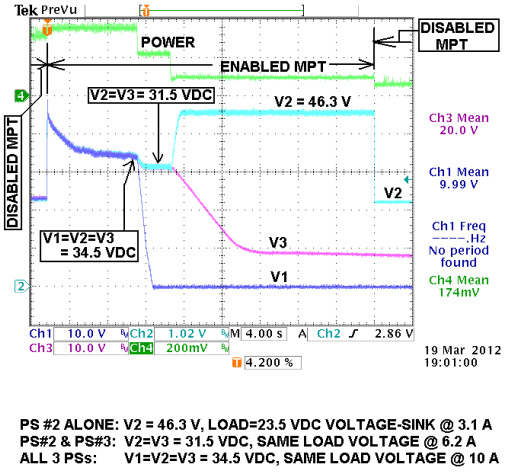

Figure 20 Prototype response during MPT mode of operation with UIVD, showing gradual transitions from three active power sources, then to two active power sources , and finally to only one active power source PS#2

Figure 21 shows the prototype response of the three input sourcing voltages and the total sourcing input power during the MPT mode of operation, revealing gradual transitions in a reverse sequence from a state of only one active power source PS#2, to a state of two active power sources PS#2 and PS#3, and finally to a state of three active power sources. Figure 21 also reveals two occasions in which the collapse of sourcing input voltages occurs when MPT of operation is disabled. One occasion is on the far left of the figure when only PS#2 is active, and another occasion is on the far right of the figure when all three power sources are active. Again, the total sourcing power under the disabled MPT mode is always less than that under the enabled MPT mode for the same number of active power sources.

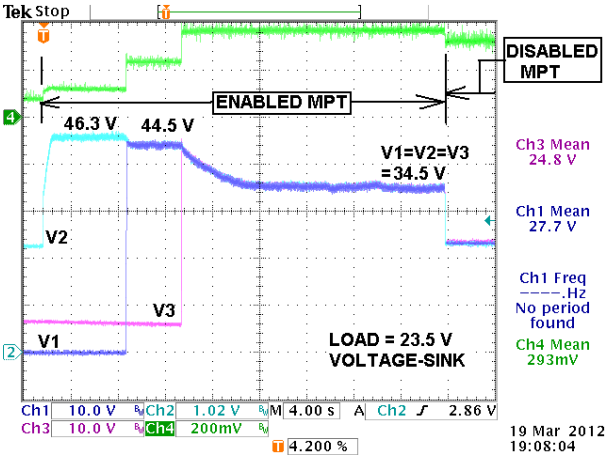

Figure 21 Prototype response during MPT mode of operation with UIVD, showing gradual transitions from only one active power source PS#2, then to two active power sources PS#1 and PS#2, and finally to three active power sources

5. Conclusion

PSPICE simulation and experimental prototype testing have validated the concept of group maximum power tracking for DIPO converter architectures using uniform input voltage distribution control. With uniform input voltage distribution control, the power delivered by the simulated power system was nearly identical to the available peak power ideally harvestable from the distributed sources. The presented power and control architecture uses a single MPT controller for all input power sources instead of dedicated MPT controllers for each input power source. Such an approach offers near-ideal MPT tracking at reduced system complexity and outstanding fault tolerances. Provided that the maximum power point voltages of the input power sources are similar, the resulting system architecture offers near-maximum power transfer with a lower parts count despite non-identical power ratings among the power sources.

6. Acknowledgment

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