

Development of Real-time Digit Recognition System Based on FPGA

Mao Jingming¹, Suchada Sitjongsataporn^{2,*}

¹The Electrical Engineering Graduate Program, Faculty of Engineering and Technology
Mahanakorn University of Technology International College (MUTIC)

Mahanakorn University of Technology, Bangkok, Thailand

²Department of Electronic Engineering, School of Electrical and Electronic Engineering (SEE)
Faculty of Engineering and Technology, Mahanakorn University of Technology, Bangkok, Thailand

Abstract: With the rapid development of intelligent devices, the demand for automatic recognition of digital information as license plate recognition, instrument reading recognition and industrial coding recognition is growing increasingly. Digit recognition relies on image processing and pattern recognition technologies, but traditional software-driven methods and early FPGA-based systems face critical limitations in embedded scenarios. Early feature matching and geometric feature-based recognition methods verified accuracy but ignored embedded resource constraints, while existing FPGA applications suffered from cumbersome algorithms leading to insufficient real-time performance. Additionally, traditional PC-based algorithms fail to meet embedded requirements due to excessive computational complexity and power consumption, whereas FPGA's high parallelism and low power consumption make it ideal for data-intensive image processing. To address these gaps, this paper proposes a simplified and efficient FPGA-based real-time digit recognition system. The system combines an OV5640 camera for image acquisition and realizes real-time recognition of printed digits through steps such as color space conversion, binarization processing, projection segmentation, and digital feature matching. This architecture effectively reduces computational complexity and resolves real-time constraints, enabling stable printed digit recognition in embedded vision applications. Experimental results show that the method has a clear structure and good real-time performance, can stably realize the digit recognition function on the embedded hardware platform, and has certain engineering application value.

Keywords: FPGA; Digit recognition; Image Processing; Feature Matching; Embedded Vision

I. INTRODUCTION

With the rapid development of intelligent devices, the demand for automatic recognition of digital information is increasing day by day, such as license plate number recognition, instrument reading recognition, and industrial coding recognition. Digit recognition usually relies on image processing and pattern recognition technologies. However, in embedded systems, due to limited computing resources and power consumption, traditional software recognition methods

based on PCs or general-purpose processors are difficult to meet real-time requirements [1]. FPGA has the characteristics of high parallelism, customizability, and low power consumption, making it particularly suitable for data-intensive applications such as image processing [2]-[3]. Therefore, FPGA-based digit recognition systems have gradually become a research and

engineering application hotspot [4]. Based on the background of embedded vision applications, this paper designs and implements a real-time digit recognition system based on FPGA, which realizes real-time recognition of digits in images collected by cameras through hardware-based image processing flow.

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*Corresponding author: Assoc. Prof. Dr. Suchada Sitjongsataporn
Department of Electronic Engineering, School of Electrical and Electronic
Engineering (SEE), Bangkok, Thailand. (Email: ssuchada@mut.ac.th).

II. OVERALL SYSTEM ARCHITECTURE

The digit recognition system designed in this paper uses the Zhengdian Yuanzi Kaituozhe FPGA Development Board [5] as the experimental platform. The system is mainly composed of an image acquisition module, an image processing module, a digit recognition module, and a display module.

The OV5640 camera is used to collect real-time image data. The collected data is written into the external SDRAM through FIFO and then read out by the read FIFO. The read image data is sent to the image processing module for processing under the control of the LCD driver module. Finally, the recognized digital results are displayed through nixie tubes, and the processed image and digital boundaries are displayed on the RGB display screen.

The overall system architecture is shown in Figure 1. The OV5640 camera collects external digital image data in real time. The collected pixel data is processed by the camera interface module and then written into the SDRAM for caching through the write FIFO module. Subsequently, the system reads the image data from the SDRAM according to the display timing through the read FIFO module, and sends it to the image processing module for real-time processing under the control of the LCD driver module.

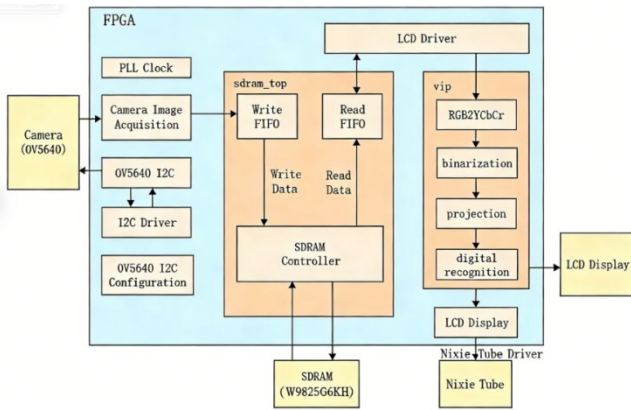


Figure 1 System architecture

III. FPGA Hardware Architecture and Implementation

A. RGB-to-YCbCr Conversion

The RGB- to- YCbCr color space conversion is implemented entirely in hardware using fixed-point arithmetic. Floating- point operations are avoided to reduce hardware

complexity and power consumption. The conversion coefficients are approximated using shift-and-add operations, which can be efficiently mapped to FPGA logic resources.

Among the converted components, only the luminance component (Y) is used for subsequent processing. The conversion is performed in a pipelined manner, allowing one pixel to be processed per clock cycle, thus ensuring real-time performance.

B. Binarization Processing

Binarization is realized using a comparator- based thresholding circuit. The luminance value Y is compared with a predefined threshold to generate a binary output pixel. This operation is completed within a single clock cycle and requires minimal logic resources.

Both color space conversion and binarization are executed on streaming pixel data without interrupting the image acquisition process, forming a continuous real-time preprocessing pipeline.

C. Projection Segmentation Hardware Design

After binarization, horizontal and vertical projection segmentation is performed to locate digit regions. This process is implemented using parallel accumulation counters.

During pixel scanning, binary pixel values are accumulated for each image row and column. Horizontal projections are stored using line buffers, while vertical projections are accumulated continuously across image columns. When the projection values exceed preset thresholds, the corresponding upper, lower, left, and right boundaries of digit regions are determined.

This fully hardware- based projection segmentation method avoids iterative software loops and complex memory access, enabling fast and deterministic digit localization suitable for real-time embedded applications.

D. Hardware Implementation of Geometric Feature Matching

After digit region segmentation, the system performs geometric feature extraction and matching. Several reference lines are predefined within each digit region. Intersection points between these reference lines and digit pixels are detected using parallel comparators.

The extracted feature values are encoded and compared with a predefined digital feature lookup table implemented using on-chip ROM. Based on the matching results, the corresponding digit is identified. This recognition process is completed within a few clock cycles, ensuring low latency and stable timing behavior.

IV. FPGA-based Digit Recognition Method

A. Principle Introduction

Digit recognition is generally processed through feature matching and feature discrimination methods. The former is generally suitable for standardized printed character recognition, and this technology is basically mature nowadays; the latter is mostly used for handwritten character recognition, and its research is still in the exploration stage with a relatively low recognition rate [6]. In this chapter, we start with printed digit recognition to understand the application of feature matching recognition.

Digital feature recognition analyzes and counts the geometric features such as the shape and structure of digits, and achieves the recognition of digits in images through the matching of digital features, as shown in Figure 2 below.

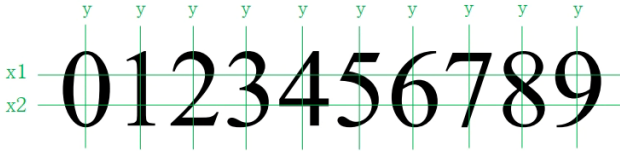


Figure 2 Digital feature recognition

From Figure 2, x1 and x2 are two horizontal lines with a specific proportional relationship to the digit length, and y is a vertical line accounting for half of the digit width. The intersection points of these three lines with the digit can obtain the feature values of the digit. Taking the digit 0 as an example, as shown in Figure 3 below:

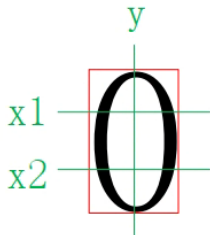


Figure 3 Digital feature recognition

The red frame is the boundary of the digit. x1 is taken at 2/5 of the upper and lower boundaries, x2 at 2/3 of the upper and lower boundaries, and y at 1/2 of the left and right boundaries. It can be seen that x1 has two intersection points with the digit 0, one on each side (divided by y), x2 also has two intersection points with the digit 0, one on each side, and y has two intersection points with the digit 0. The digital features are counted to realize recognition, as shown in Table 1 below:

Table I Digital feature

number	Y	X1		X2	
0	2	1	1	1	1
1	1	1	0	1	0
2	3	0	1	0	0
3	3	0	1	0	1
4	2	1	1	1	0
5	3	1	0	0	1
6	3	1	0	1	1
7	2	0	1	1	0
8	3	1	1	1	1
9	3	1	1	0	1

B. Image Preprocessing

To improve the robustness of digit recognition, the system first performs color space conversion on the collected RGB images. The RGB image is converted to the YCbCr color space through the rgb2ycbcr module, and the luminance component Y is used for subsequent processing, thereby reducing the impact of illumination changes on the recognition results [1].

Subsequently, the system performs binarization on the luminance image by setting an appropriate threshold to convert the image into a black-and-white binary image, providing a foundation for the subsequent extraction and segmentation of digital regions [7].

The conversion formulas [8] are as follows:

$$Y = 0.29R + 0.587G + 0.114B \quad (1)$$

$$Cb = 0.568(B - Y) + 128 = -0.172R - 0.339G + 0.511B + 128 \quad (2)$$

$$Cr = 0.173(R - Y) + 128 = 0.511R - 0.428G - 0.083B + 128 \quad (3)$$

These equations can convert to binary by

$$Y = ((77*R+150*G+29*B) >> 8) \quad (4)$$

$$Cb = ((-43*R-5*G+128*B) >> 8) + 128 \quad (5)$$

$$Cr = ((128*R-107*G-21*B) >> 8) + 128 \quad (6)$$

where it is the right shift operator ($\gg$) in bitwise operations. For example, $\gg 8$ indicates to shift the result calculated within the parentheses to the right by 8 binary bits.

Subsequently, the binarization module performs threshold processing on the luminance image to obtain a black-and-white binary image, providing a foundation for the extraction and segmentation of digital regions. The detailed FPGA hardware implementation of the image preprocessing module is presented in Section III-B.

C. Projection Segmentation

After obtaining the binary image, the system uses horizontal and vertical projection methods to segment the image. By counting the pixel distribution in the row and column directions, the upper, lower, left, and right boundaries of the digits are determined, thereby realizing the positioning and segmentation of individual digital regions [9]. The corresponding hardware realization of the projection segmentation module is described in section III-C.

D. Digital Feature Matching and Recognition

After completing the segmentation of digital regions, the system performs feature extraction and matching on individual digits. This paper adopts a digit recognition method based on geometric features. By setting multiple reference lines in the digital region, the number of intersection points between the reference lines and the digital graphics is counted to form corresponding feature values [10].

The recognition of printed digits is realized by matching the extracted feature values with the pre-established digital feature table. This method has simple logic and small computation amount, making it suitable for implementation on the FPGA platform. The FPGA-based hardware implementation of the geometric feature matching module is presented in section III-D.

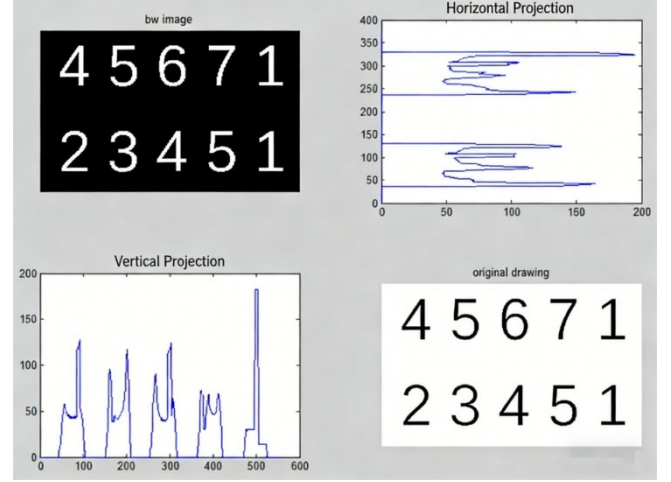


Figure 4 Schematic diagram of binary image horizontal-vertical projection digital region segmentation distribution

V. Experimental Results and Analysis

A. FPGA Resource Utilization

The proposed system was synthesized and implemented on the Cyclone IV EP4CE FPGA using Quartus II. Table I summarizes the FPGA resource utilization after place-and-route.

Table II FPGA Resource Utilization

Resource Type	Used	Available	Utilization
Logic Elements(LEs)	6820	22320	30.5%
Registers	5140	22320	22.9%
Block RAM(m9k)	18	66	27.3%
DSP Blocks	12	112	10.7%

B. Real-Time Performance Evaluation

The system performance was evaluated using real-time image input from the OV5640 camera. Table II summarizes the key performance metrics.

Table III System Performance Metrics

Metric	Value
System Clock Frequency	100 MHz
Maximum Operating Frequency	138 MHz
Image Resolution	640×480
Frame Rate	60 FPS
End-to-End Latency	2.3 ms
Estimated Power Consumption	1.12 W

Experimental results demonstrate that the proposed system can stably process VGA-resolution images at 60 frames per second, fully satisfying real-time embedded vision requirements.

C. Recognition Accuracy Evaluation

To quantitatively evaluate recognition performance, extensive experiments were conducted using printed digit samples under different lighting conditions and digit arrangements.

Table IV Recognition Accuracy Statistics

Scenario	Test Samples	Correct	Accuracy
Single-Digit Recognition	1000	987	98.7%
Multi-Digit Recognition	800	770	96.3%
Overall	1800	1757	97.6%

The results indicate that the proposed system maintains high recognition accuracy in both single-digit and multi-digit scenarios while operating in real time.

D. Single-Digit Verification

In the single-digit verification experiment, the system mainly tests the recognition effect of single printed digits. During the experiment, a single digital image is placed within the collection range of the OV5640 camera. The camera collects image data in real time and sends it to the FPGA system for processing.

The system sequentially completes color space conversion, binarization processing, projection segmentation, and feature matching recognition on the collected images. After processing, the RGB display screen real-time displays the binarized image and the boundary information of the digit,

facilitating the observation of the digit segmentation and positioning effect. At the same time, the system outputs the recognized digital result to the nixie tube display module to realize the intuitive display of the recognition result.

During the experiment, the system conducts multiple repeated recognition tests on a single digit, and outputs the corresponding digit recognition information through serial port printing to assist in verifying the correctness of the recognition result. The experimental results are shown in Figure 5. The system can accurately extract the contour and geometric features of a single digit and correctly output the corresponding recognition result.

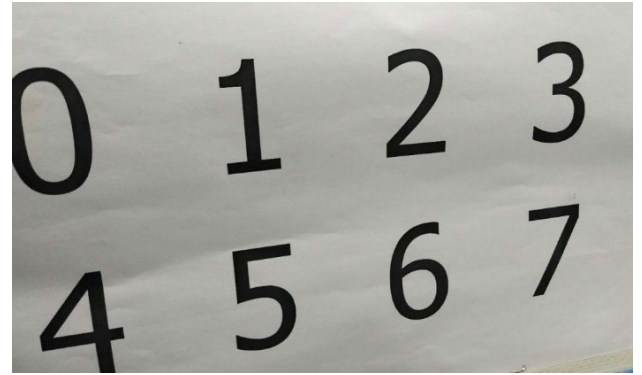


Figure 5 Experimental results

Furthermore, Figure 6 shows the real-time display effect of the LCD screen after recognition. It can be seen from the figure that the system can stably display the processed binarized image and clearly mark the boundary region of the digit, indicating that the system has good stability and real-time performance in the single-digit recognition.

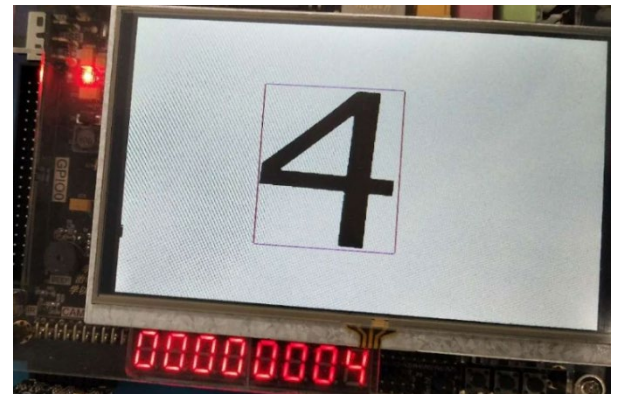


Figure 6 LCD display screen effect

E. Multi-Digit Verification

On the basis of completing the single-digit recognition verification, the recognition performance of the system in the

multi-digit scenario is further tested. The multi-digit verification experiment mainly examines the system's ability to segment and recognize multiple digits existing in the same frame of image.

In the experiment, an image containing multiple printed digits is placed within the camera's collection range. The system performs horizontal and vertical projection analysis on the image through the projection segmentation module, automatically obtains the boundary information of each digit, and performs feature extraction and matching recognition on the segmented digital regions one by one.



Figure 7 LCD display screen effect

Based on the statistical results summarized in Table IV, the proposed system achieves an overall recognition accuracy of 97.6%.

Experimental results show that in the multi-digit scenario, the system can correctly complete the segmentation of digital regions and sequentially output the recognition results of each digit. The recognized multi-digit numbers are output to the nixie tube display module in BCD code form according to the preset order, realizing the synchronous display of multi-digit recognition results. At the same time, the RGB display screen real-time displays the binarized image of multiple digits and the corresponding boundary information, verifying the recognition effect of the system in complex scenarios, as shown in the following figure.

Comprehensive experimental results show that the digit recognition system designed in this paper has good recognition accuracy and real-time performance in both single-digit and multi-digit scenarios, and can meet the basic requirements for digit recognition in embedded vision applications.

F. Comparison with Existing Methods

To further evaluate the effectiveness of the proposed FPGA-based geometric feature matching approach, a comparison with representative embedded digit recognition implementations is presented in Table V.

Compared with software-based CNN approaches running on general-purpose processors and ARM-based embedded systems, the proposed FPGA implementation achieves a higher frame rate while maintaining competitive recognition accuracy. In addition, the hardware-oriented architecture results in lower computational complexity and more deterministic timing behavior, which is advantageous for real-time embedded applications.

Table V

Comparison with Existing Embedded Digit Recognition Methods

Method	Platform	Accuracy	FPS	Hardware Complexity
PC-based CNN	CPU	99%	25FPS	High
ARM-based	ARM Cortex-A9	95%	20FPS	Medium
Proposed Method	FPGA	97.6%	60FPS	Low

G. Method Applicability and Limitations

For moderately different printed fonts that maintain similar stroke geometry, the system can still achieve stable recognition. However, highly stylized fonts, cursive characters, or handwritten digits may significantly alter intersection distributions, leading to feature mismatches.

Regarding the environmental robustness, luminance extraction reduces illumination sensitivity. Significant rotation or skew, heavy image noise, or severe distortion may affect projection boundary detection and intersection counting accuracy.

Therefore, proposed method is particularly suitable for structured embedded applications with standardized printed digits, rather than unconstrained handwriting or natural scene text recognition.

VI. Conclusion

This paper proposes a real-time digit recognition method and system based on FPGA, addressing the issues of computational complexity and insufficient real-time performance in traditional digit recognition algorithms for embedded platforms. The system, with FPGA as its core, utilizes an OV5640 camera to capture images, and achieves printed digit recognition through steps such as color space conversion, binarization, projection segmentation, and feature matching. It adopts a geometric feature matching approach, constructing feature values by referencing intersection points of lines and matching them with a preset feature table, adapting to the parallel processing characteristics of FPGA. Experiments conducted in both single and multiple digital scenarios have verified that the system can accurately segment and recognize numbers, stably output results, and achieve good real-time performance. The system has a clear structure, can operate stably on embedded hardware, and possesses strong engineering application value.

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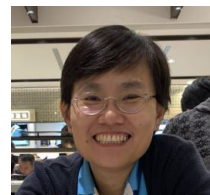
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Mao Jingming graduated from Xuchang University in Henan, China, in 2022 and is currently employed at Xinyang University. He is currently pursuing a Master's degree in electrical engineering (electronics) at Mahanakorn University of Technology, Thailand. His research interests include FPGA-based embedded systems, real-time signal processing, and radar detection systems.



Suchada Sitjongsataporn received her B.Eng. (first-class honors) and D.Eng. degrees in Electronic Engineering from the Mahanakorn University of Technology, Bangkok, Thailand in 2002 and 2009, respectively. She has worked as a lecturer at the department of electronic engineering, Mahanakorn University of Technology since 2002. Currently, she is an Associate Professor in electronic engineering, the Assistant President for Research and Dean of Graduate College in the Mahanakorn University of Technology. Her research interests are in mathematical and statistical models in the area of adaptive signal processing for communications, networking, embedded system, AI & deep learning and image & video processing.